Wireless Innovation Forum 2010:
Radio Waveform Development System

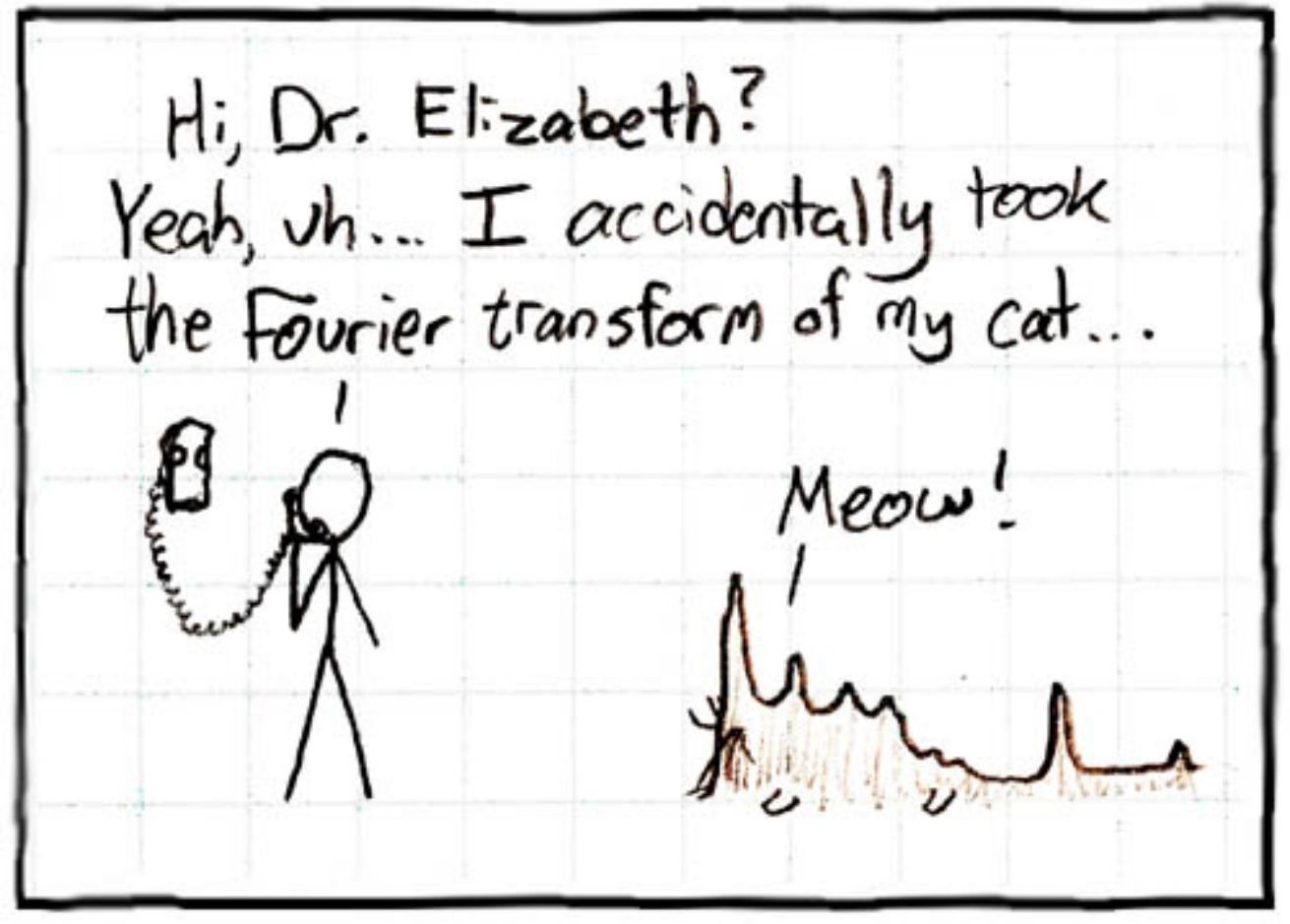
Nirali K. Patel

Kevin A. Shelby

Brian A. Dalio, Ph.D.

Photo Courtesy NASA

From xkcd.com



Objective with *an* RWDS

Place real-time hardware in the hands of the system designer:

- *Versed in C, Matlab, Simulink, …*
- *Accustomed to expressing waveform signal processing at a layer of abstraction above the HW implementation*

Agenda

- **Waveform Development Process**
  - PHY Specification
  - System Architecture
  - Design Implementation
  - Performance Characterization
- **Radio Waveform Development System (RWDS)**
  - System Architecture
  - System Configuration
- **Waveform Development**
  - Software Development Environment
  - Library Elements
  - Model Based Design Flow (MBDF)
  - Real-Time Analysis
- **Reference Waveform Implementation**
- **Closing Remarks**
- **Q&A**

Waveform Development Process

Overview

Waveform Development Process

PHY Specification is principally concerned with description of the transmitter:

- **Unambiguously describes:**
  - frame structure, multiplexing arrangement, symbol timing;
  - modulation and coding, interleaving, scrambling, (pulse shaping);
  - PHY procedures, e.g. synchronization, power control, access methods;
- **May additionally provide nominal guidelines regarding:**
  - Expected receiver performance accounting for attainable noise figure and tolerable implementation loss to achieve a given link budget/link margin.

Waveform Development Process

System Architecture determines a mapping from PHY spec to design implementation:

- **Begins with a comprehensive assessment of the system operating parameters w.r.t.:**
  - TX PHY spec conformance,
  - RX design tradeoffs to meet performance objectives, e.g. rate/range characteristics, error resilience, impairments mitigation.
- **Specifies how data rate is derived in each operating mode to satisfy a prescribed link budget:**
  - Frame structure, multiplexing arrangement, modulation and coding schemes;
  - Determines processing throughput and latency requirements
- **Enables preliminary algorithm development with ongoing refinement throughout design implementation.**

Waveform Development Process

Design Implementation entails:

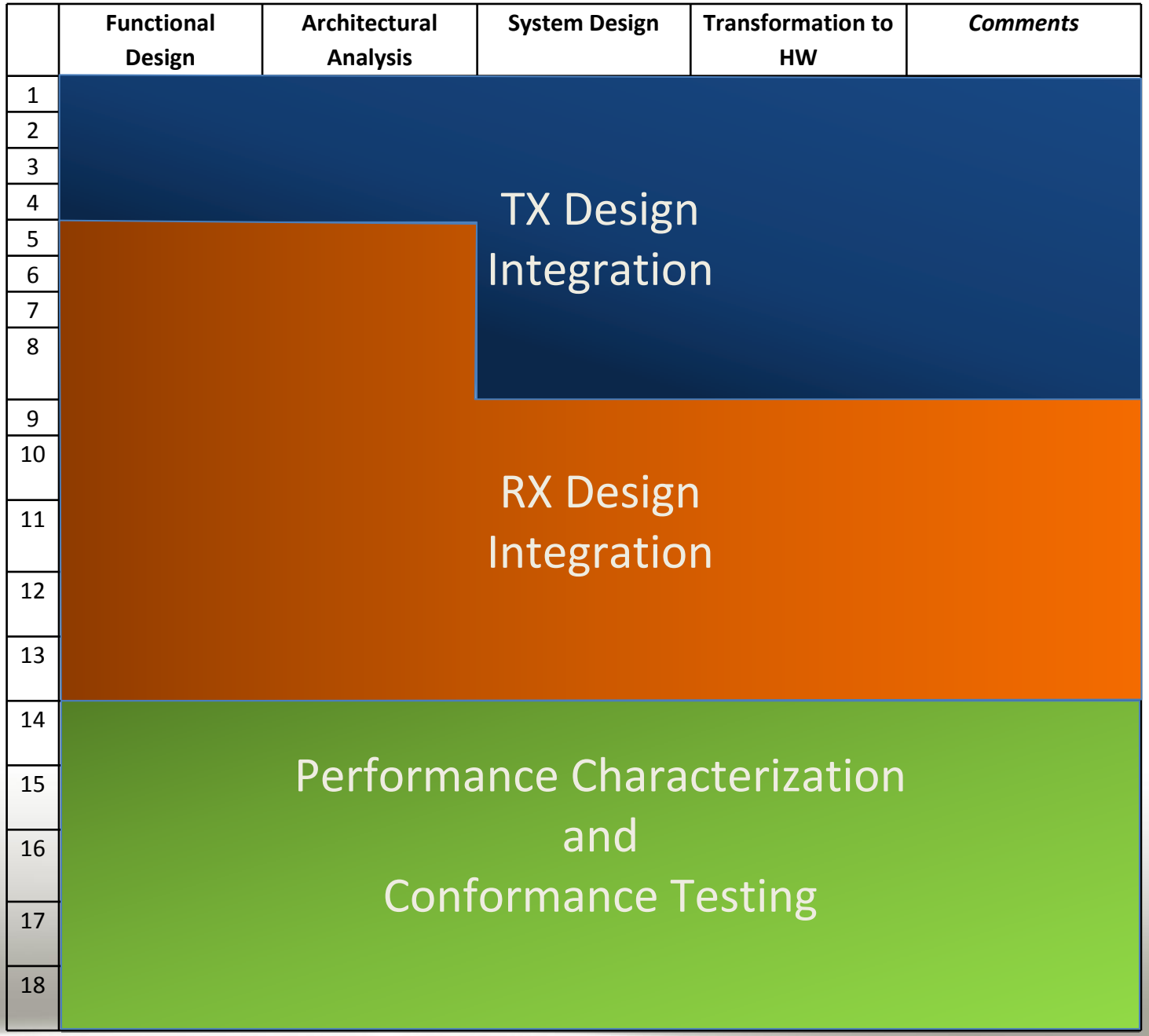
- **Functional Modeling**
- **Design verification:**
  - Test vector comparison w.r.t. TX functional model;
  - block by block RX comparison against TX inputs.
- **Data Flow and Resource Estimation**
- **Library Design, Design Integration and Resource Assignment**
- **Resource Mapping and Design Optimization**

Waveform Development Process

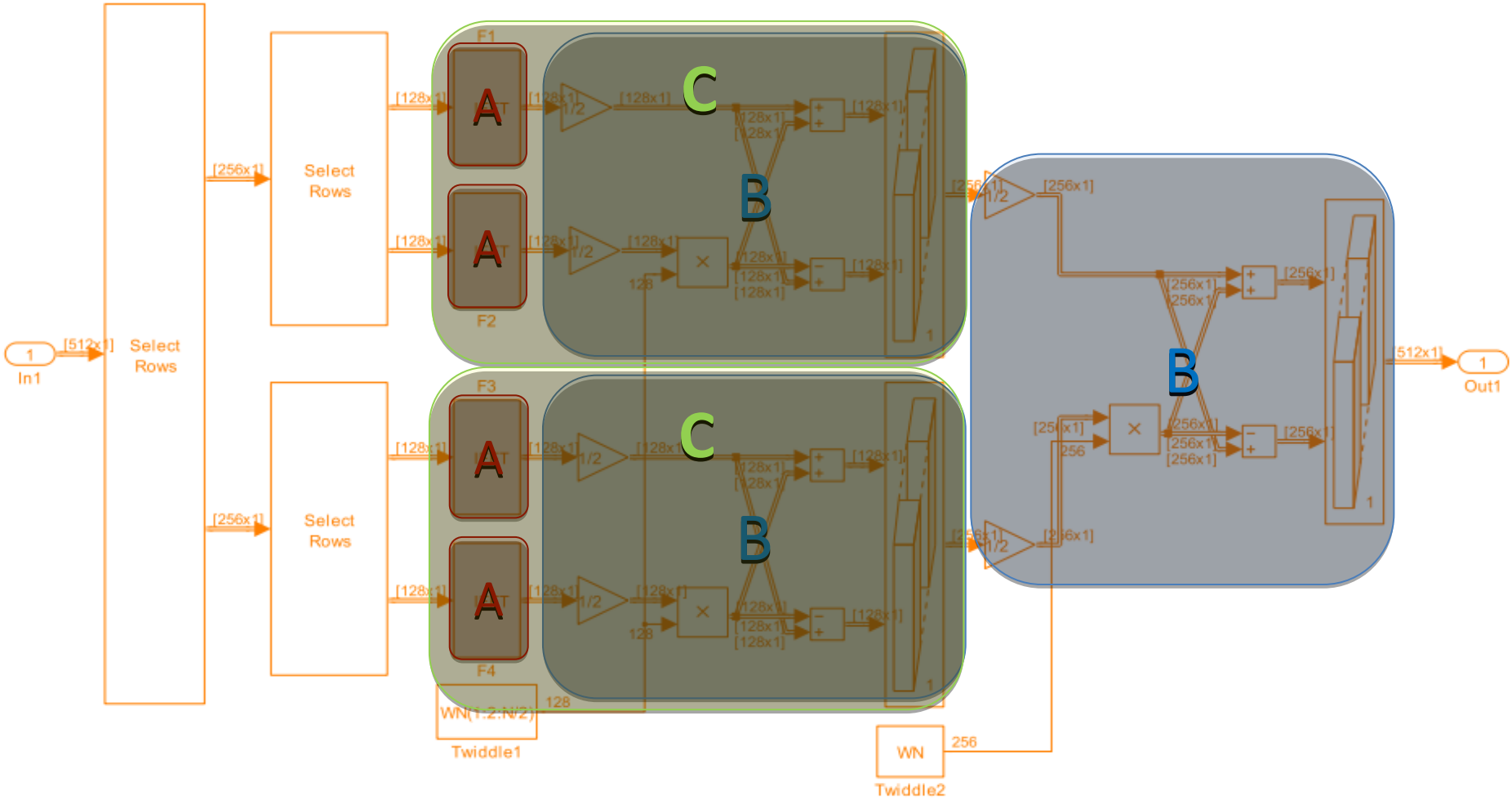
Conformance Testing and Performance Characterization:

- **Spec Compliance:**
  - TX: EVM, Power Spectral Density (PSD), Adjacent Channel Leakage Ratio (ACLR);
  - RX: Minimum Sensitivity, Implementation Loss (IL), Link Margin (LM), Multipath mitigation, CFO compensation;
  - Real-time characterization in the presence of actual system impairments, e.g. data converters, RFFE;
- **Interoperability Testing (IOT):**
  - Acquisition, sync and tracking against unaffiliated TX|RX design or representative test equipment;
  - BER/BLER performance under various channel conditions.
- **Final resource allocation and measured power dissipation.**

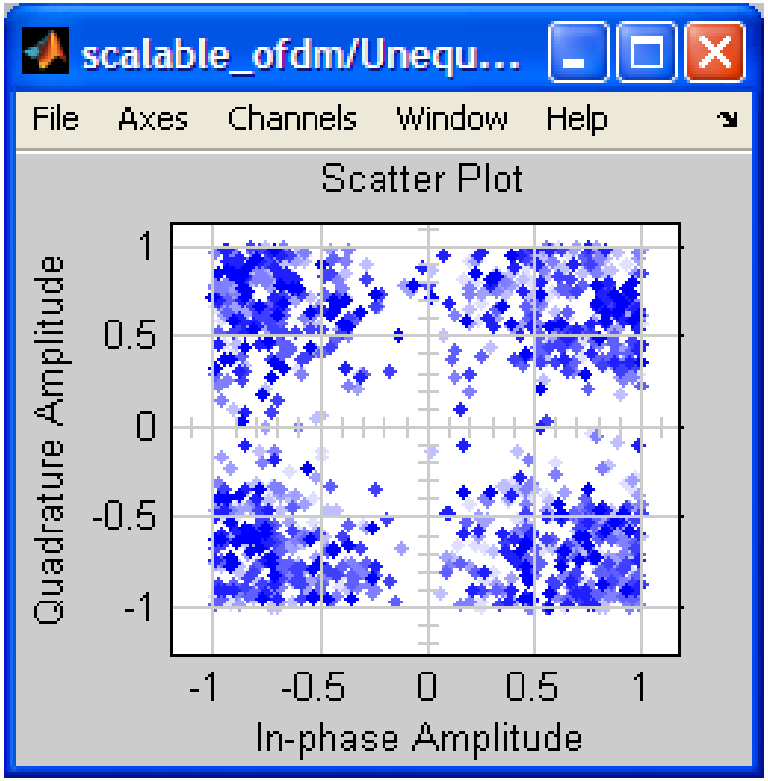
•Design Imple-mentation

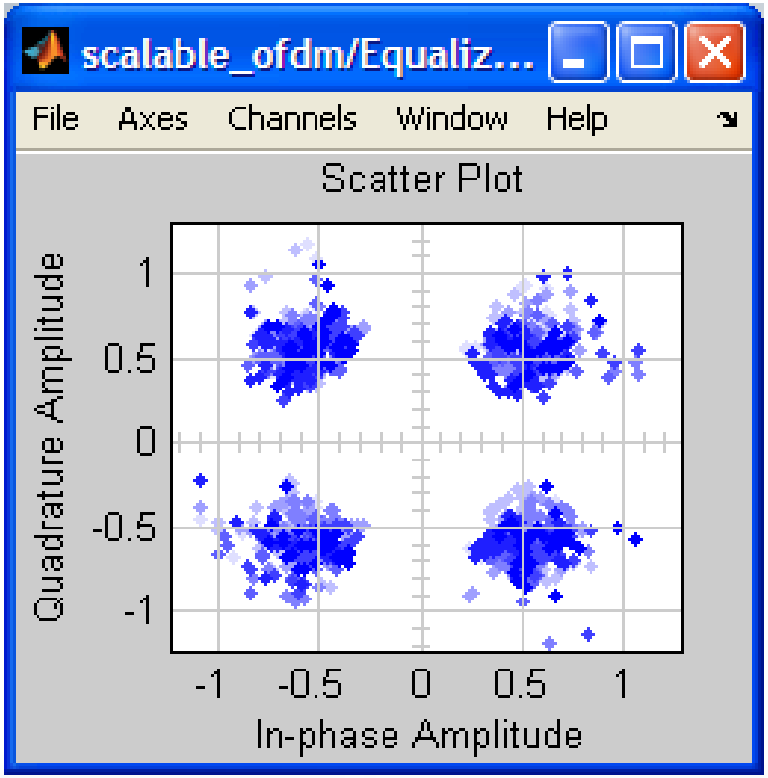


Design Partitioning



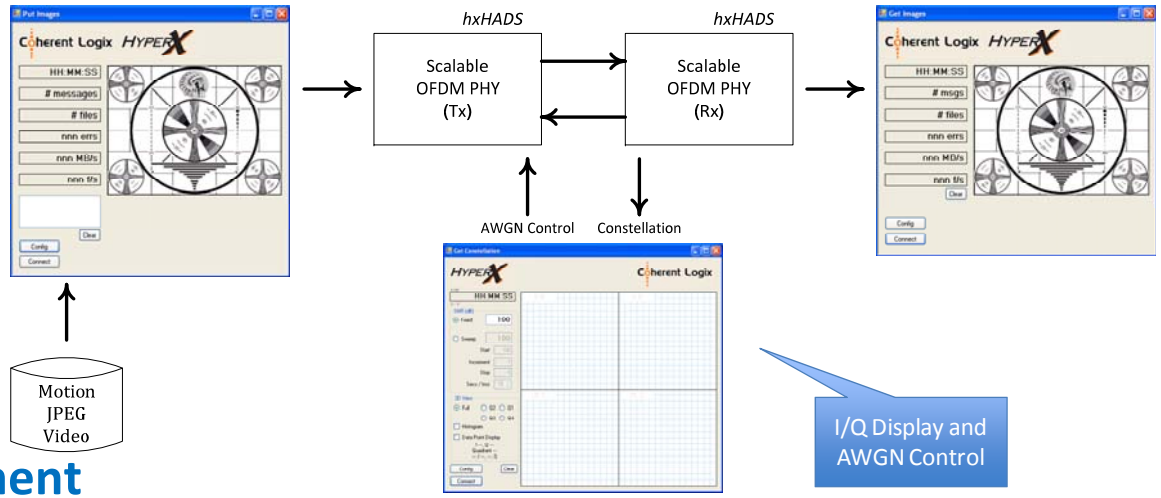
Finite Precision Requirements

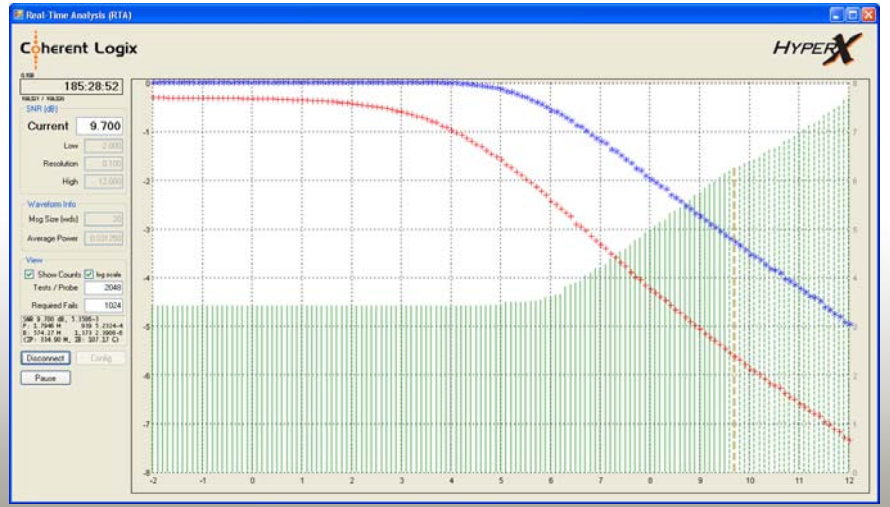




Real-time performance evaluation

- **Evaluate**
  - Functionality
  - Throughput/latency
  - Power performance
  - "Characterization" (domain specific)
- **as early in the development process as possible.**
- **Evaluate *continuously* throughout the design process.**
  - Video in … over channel … Video out
  - TX|RX Constellations
  - BER|BLER Characterization
  - Real-Time Channel Emulator

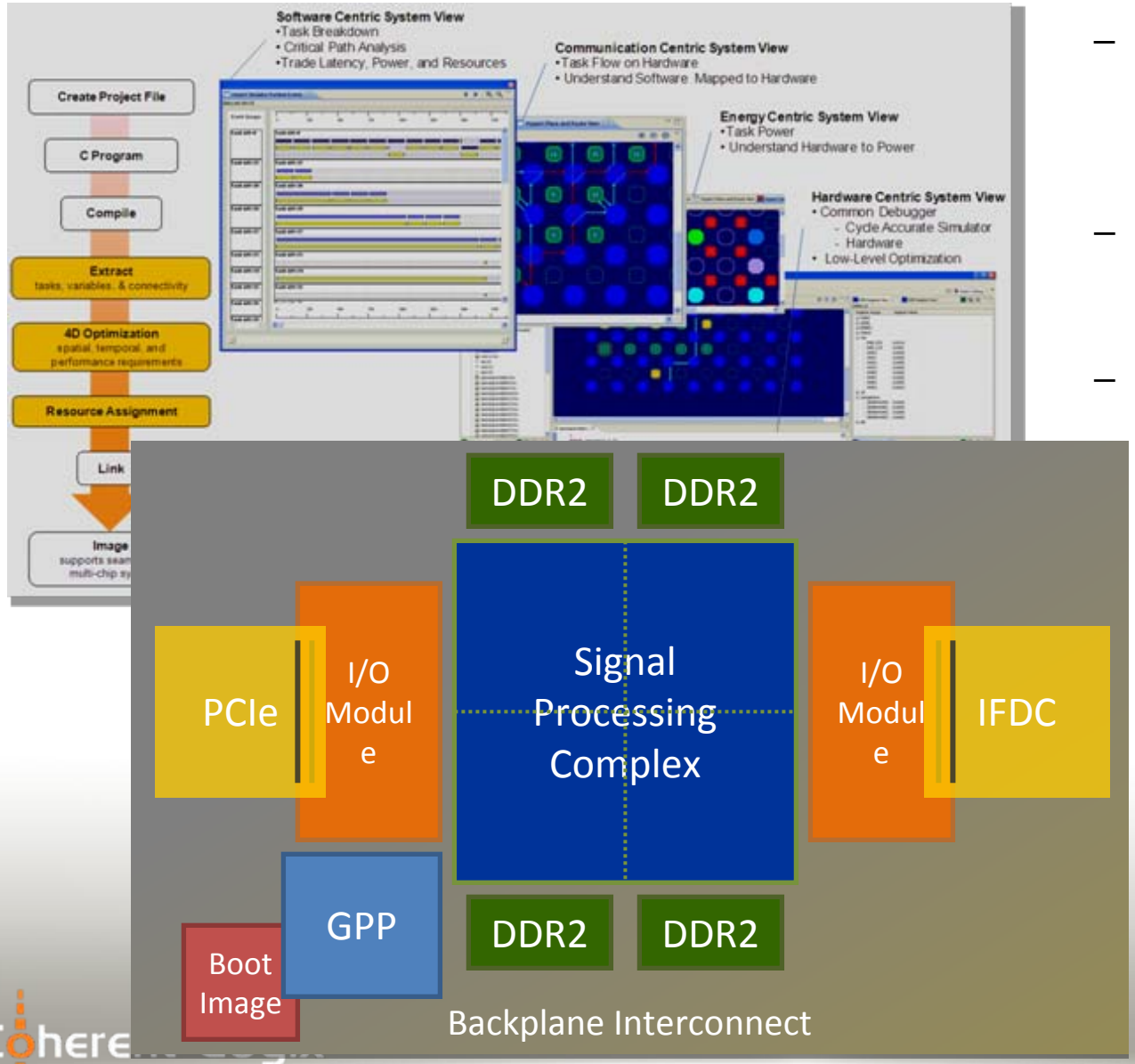




RWDS

System Architecture

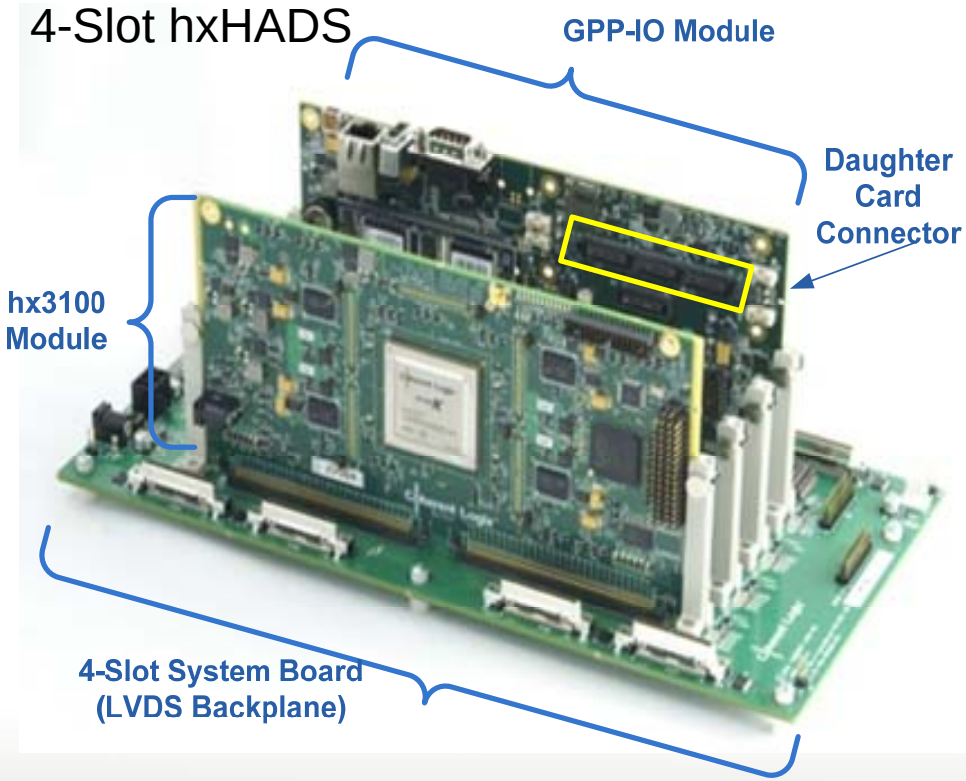
RWDS: System Architecture



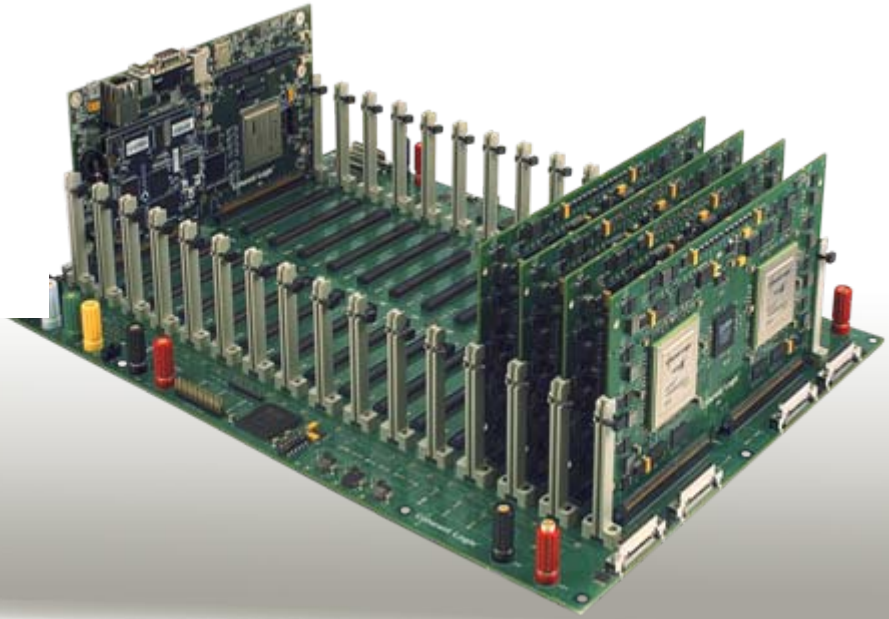
- Supports functional verification, system analysis and performance characterization at speed
- Integrated hardware development environment increases designer productivity
- Configurability supported throughout the system architecture by means of
  - The hx3100™ Programmable Signal Processing Complex
  - Modular extensibility of the hardware platform
  - Potential to add signal processing modules within reach of a single RWDS backplane

hxHADS: Hardware Application Development System

4-Slot hxHADS

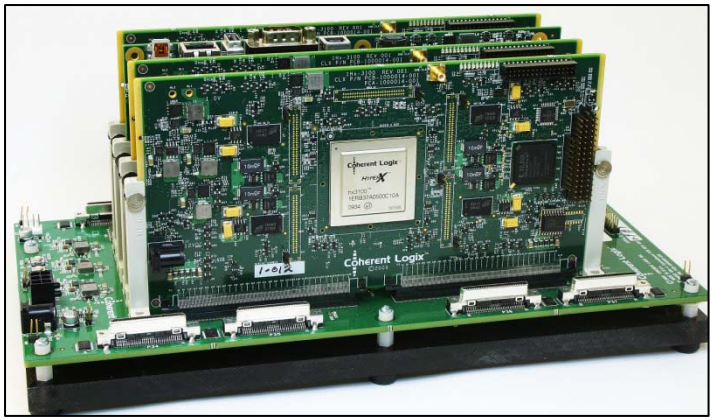


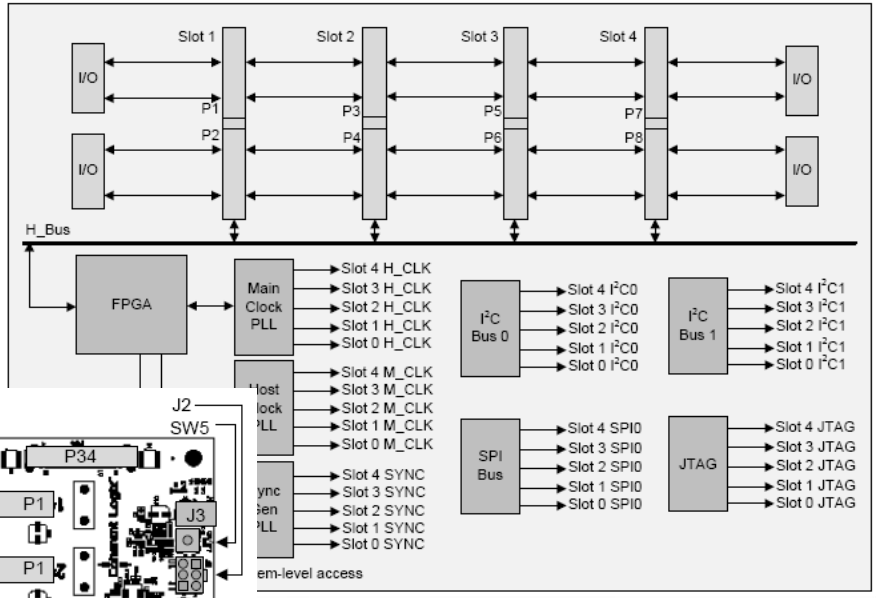
16-Slot hxHADS

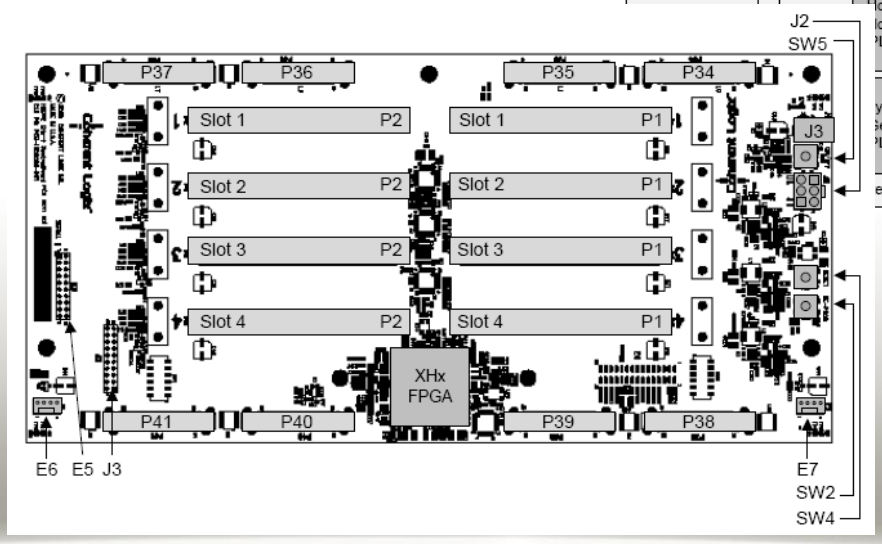


hxHADS: System Module

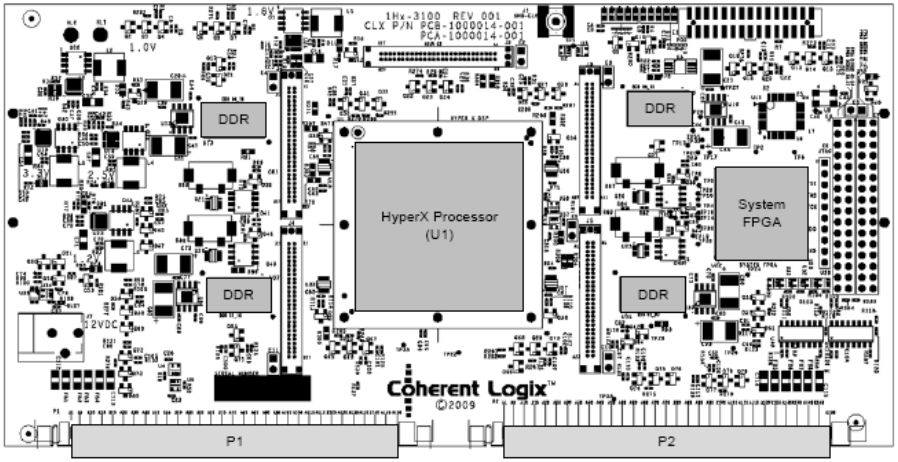
- 300 pins per connector
- 500 MHz LVDS through connector
- Bi-directional LVDS from/to 1 / 2 hx Module (customizable to LVDS / CMOS elsewhere)
- Power provided through connector

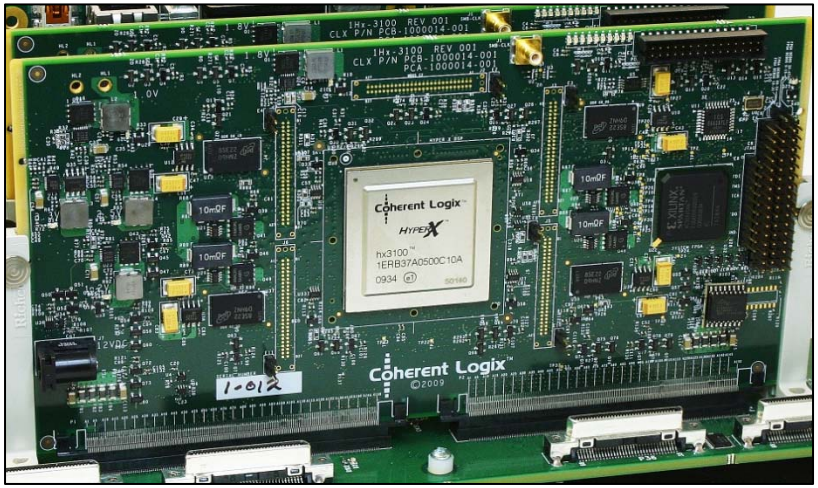






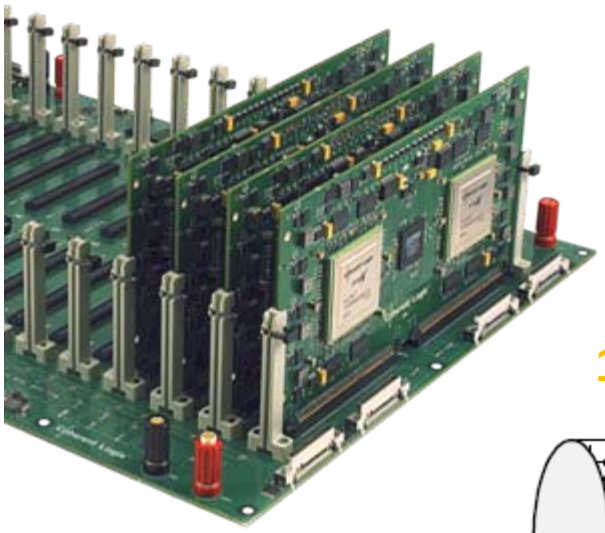
hxHADS : hx3100 Module

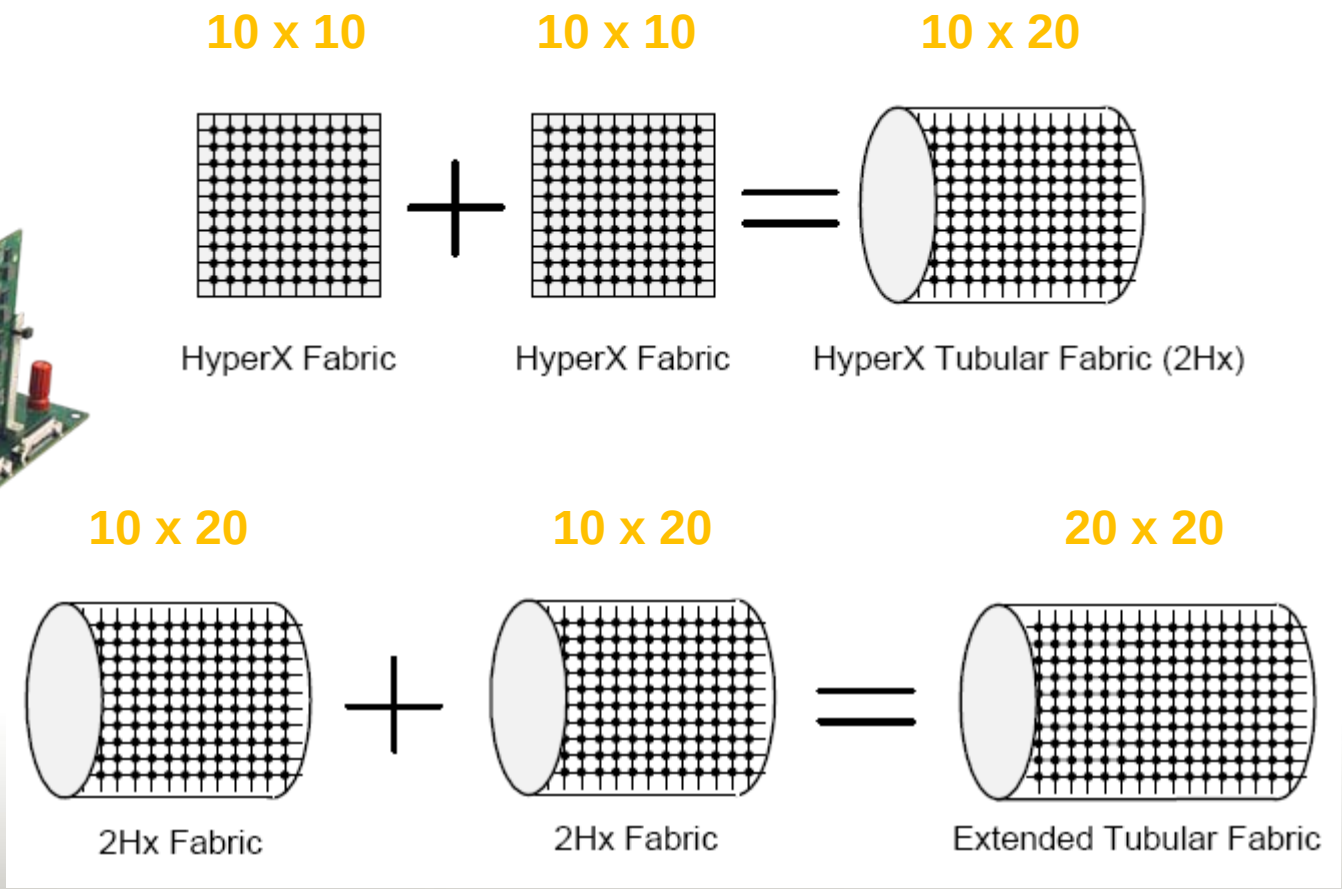




- **Instrumented to measure power on chip for core power and I/O power domains**
- **Seamlessly extend fabric via multiple hx Modules**
- **Support high-performance computing across many chips**

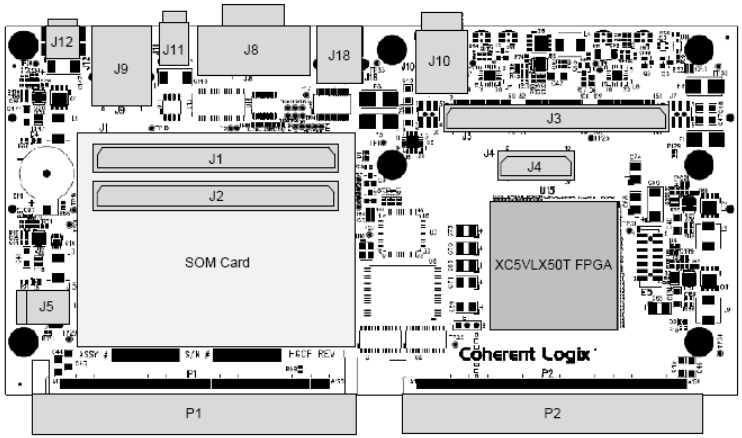
hxHADS: Extensibility with System Module

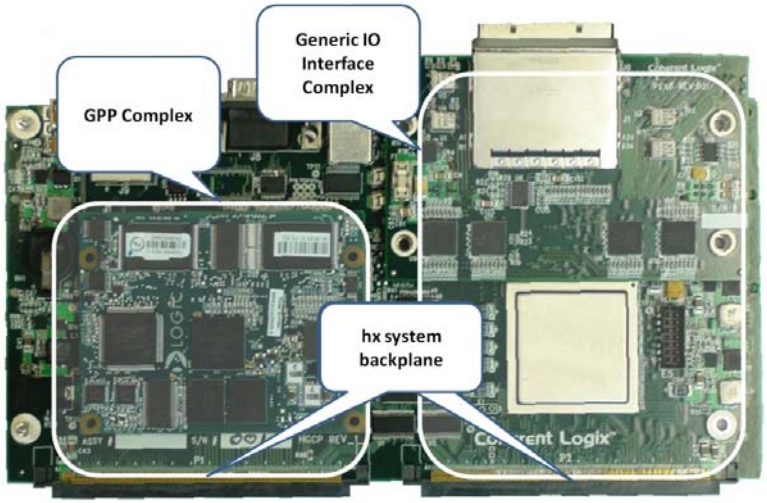


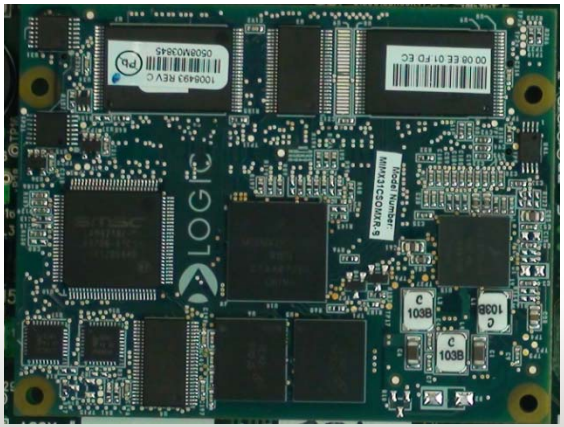


and so on …

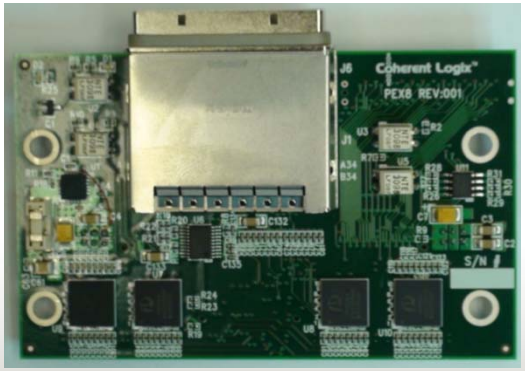
hxHADS: GPP-IO Module







GPP SOM Card (i.MX31)



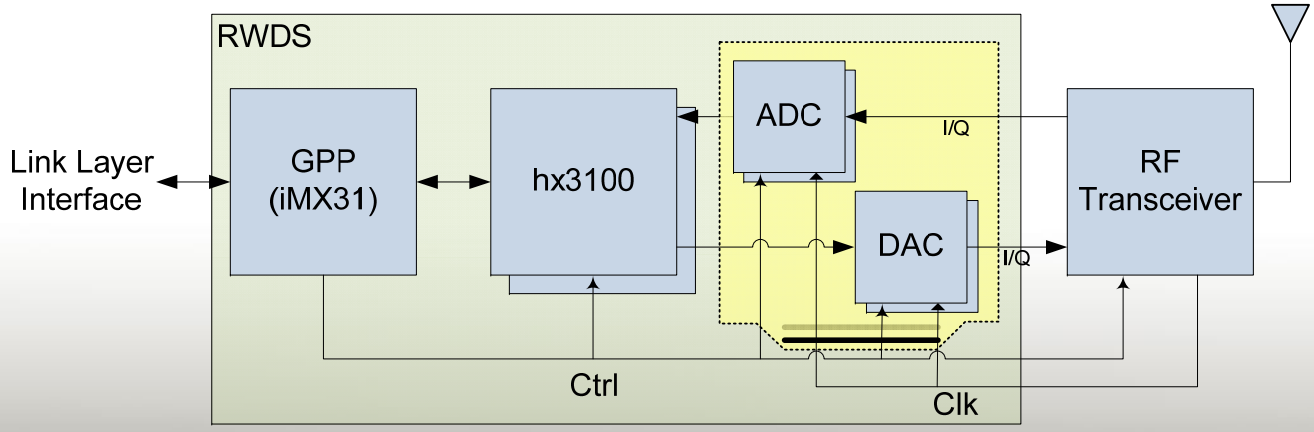
IO Adaptor Card (PCI Express)

RWDS

System Configuration

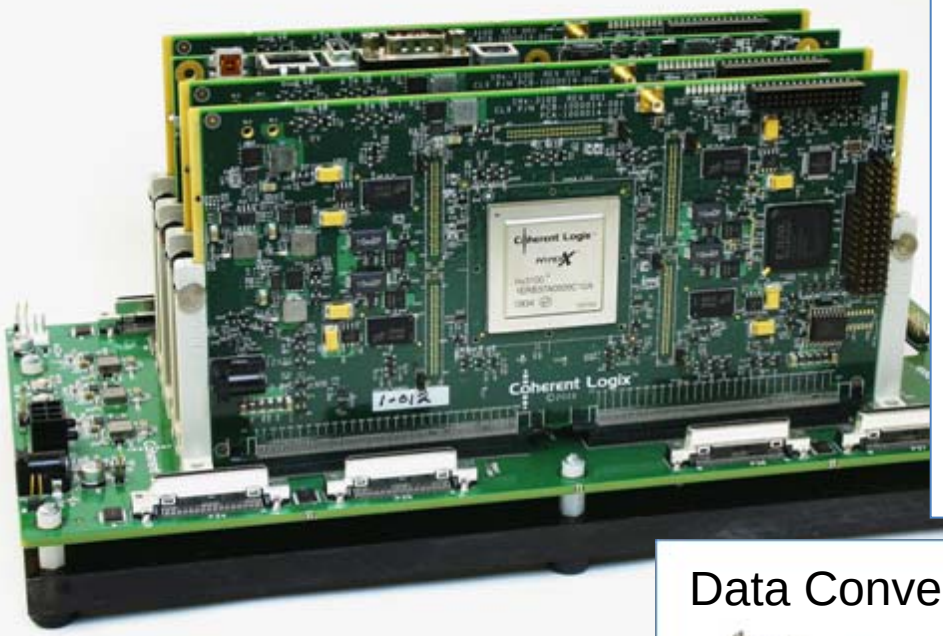
RWDS: System Configuration

- **Software Defined Radio (SDR) approach:**
  - Programmable Signal Processing Complex – performs majority of the waveform processing (e.g. modulation/ demodulation, scrambling/de-scrambling, FEC encoding/decoding, frame packing/unpacking and digital up/down conversion including resample filtering) and portions of the IF conversion
  - Configurable Radio Front End – frequency translation between RF/IF domains
  - ADC/DAC Interfaces – operated at a common IF
  - General Purpose Processor (GPP) – enables system configuration and provides the operating environment including mechanisms to define application waveforms.



RWDS: System Components

hxHADS

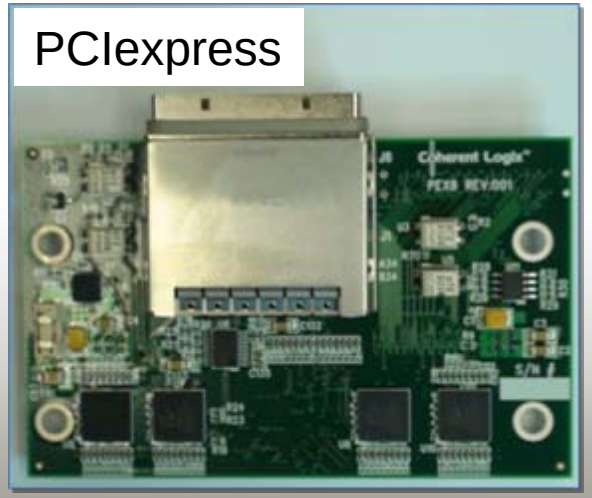


- **Built around the hxHADS**
- **Fully modular and customizable**
- **Plug-and-play capability with the HyperX ISDE**
- **Clear path to form factor product**
- **Supports**
  - PCI Express
  - Data Conversion
  - RF Front Ends

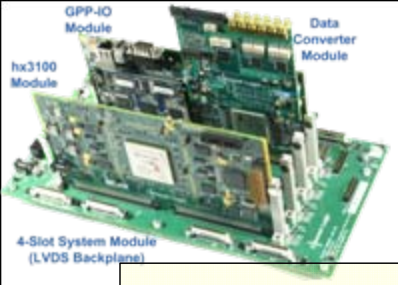
RF Front End

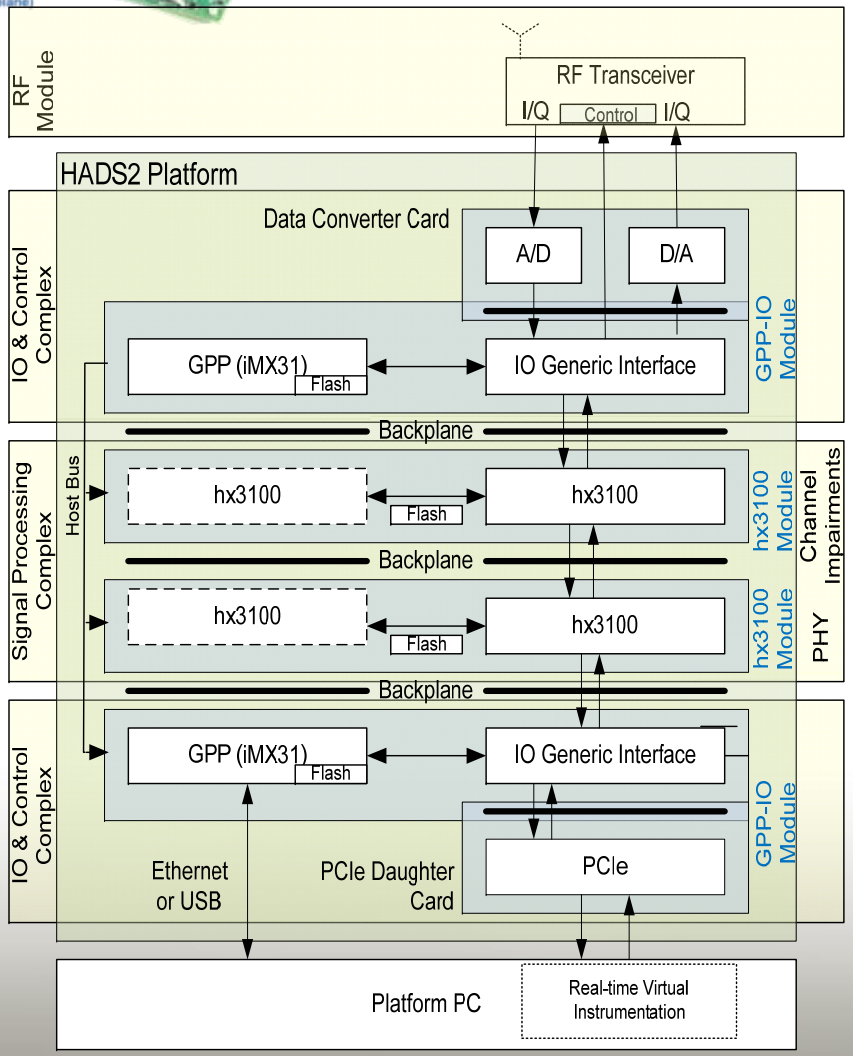
Data Converter

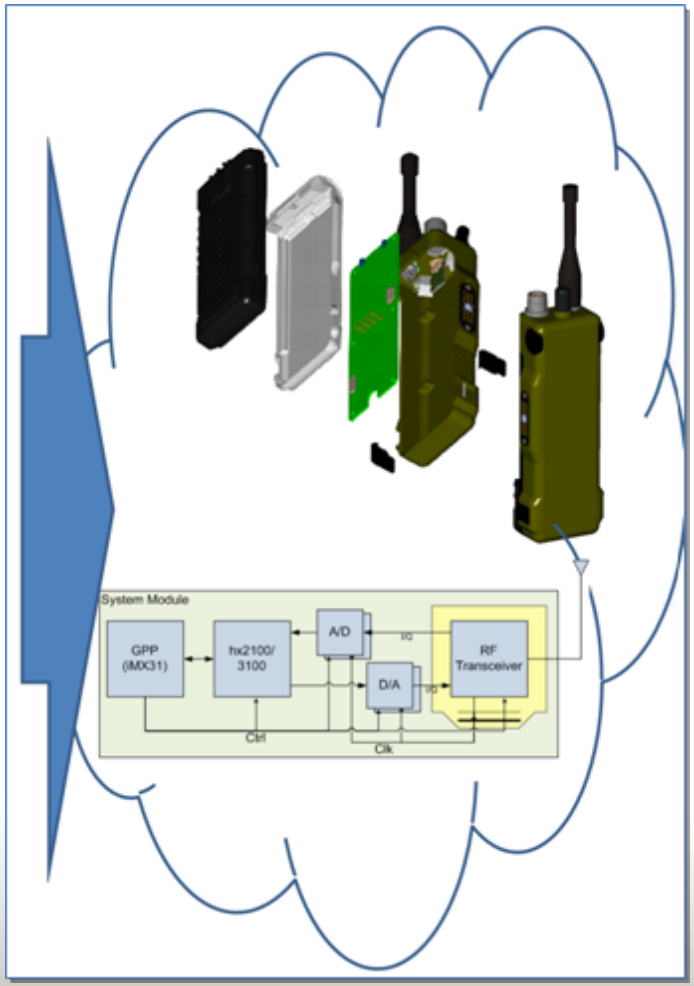
PCIexpress



RWDS: Application Waveform Mapping



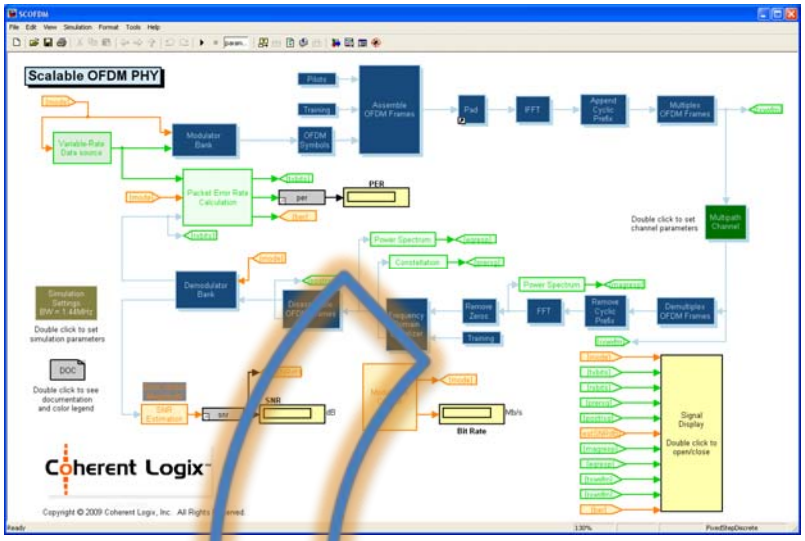


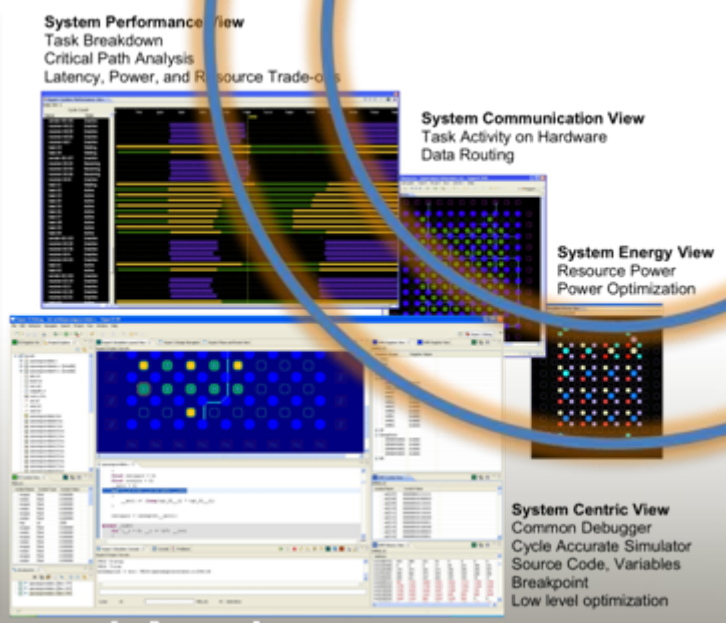


Waveform Application Development

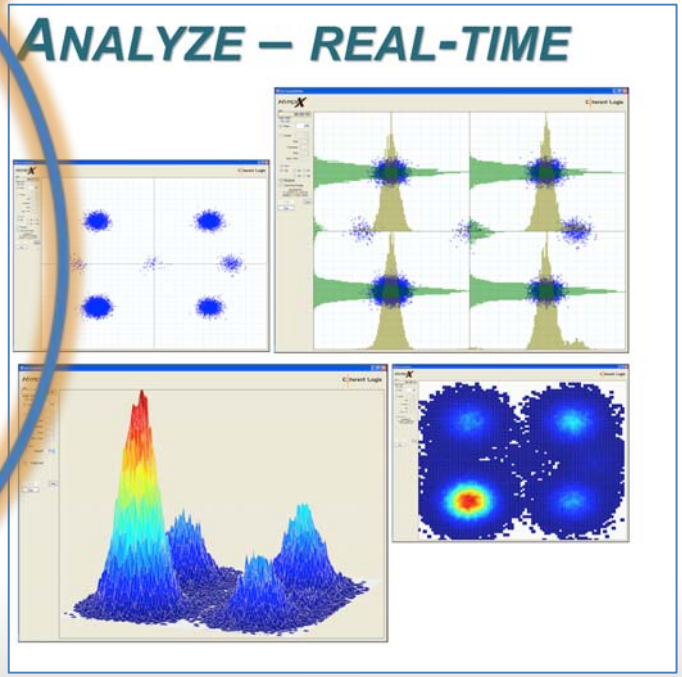
Development Environment

RWDS: Software Development Environment



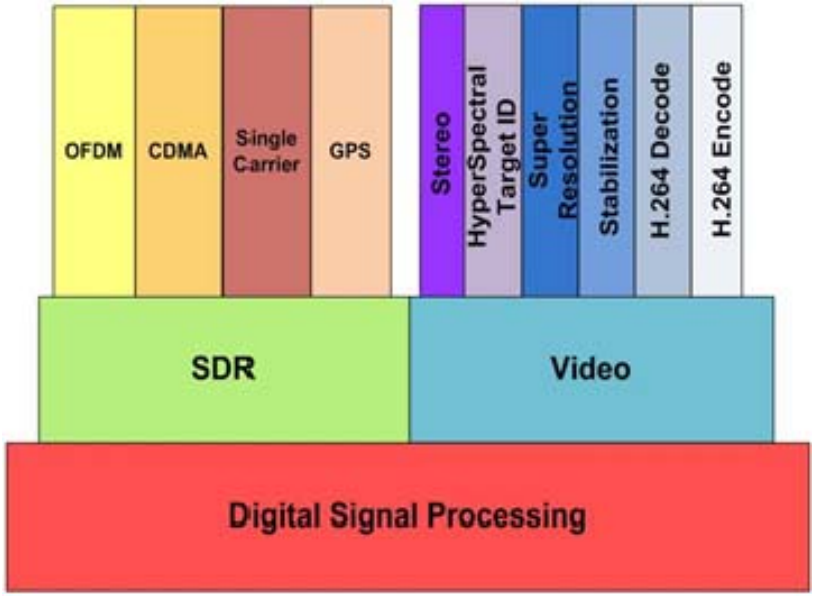


- **Parallel programming methodology**
  - Built on proven HyperX ISDE
    - ANSI-C
    - Source code platform independent until compile time
    - > 5x reduction in development time over current (DSP/FPGA)



  - Unified development and verification flow
  - Design optimizations (e.g., trading performance, power, and latency) performed without changing C code
  - Model Based Development Flow (MBDF)

Library Elements



DSP

- FFT/IFFT
- Auto-/cross-correlation
- Interpolation
- Decimation
- Adaptive Filtering
- Trend Removal
- Averaging
- Sequence generation

SDR

- CRC
- FEC
  - CC, RS-CC
  - CTC, BTC
  - LDPC
- (De-)Interleave
- (De-)Scramble
- Log Likelihood
- Synchronization
- Pulse shaping/windowing

OFDM

- Tone Mapping
- CP Insertion/ Removal
- CE/EQ
- CFO Est./ Tracking

CDMA

- (De-)Spreading
- Channel Est.
- Rake Receive
- Carrier Tracking

Single Carrier

- (PR-)CPM, PAM, MSK
- Pulse Decomposition
- Linear EQ
  - Time/Freq domain
- Trellis EQ/Demod
- Turbo EQ

Satellite Navigation

- I/FFT Acquisition
- P-Code generator
- Code Phase Tracking (DLL)
- Carrier Phase Tracking (PLL)
- Direct P-Code Acquisition w/ dual folding

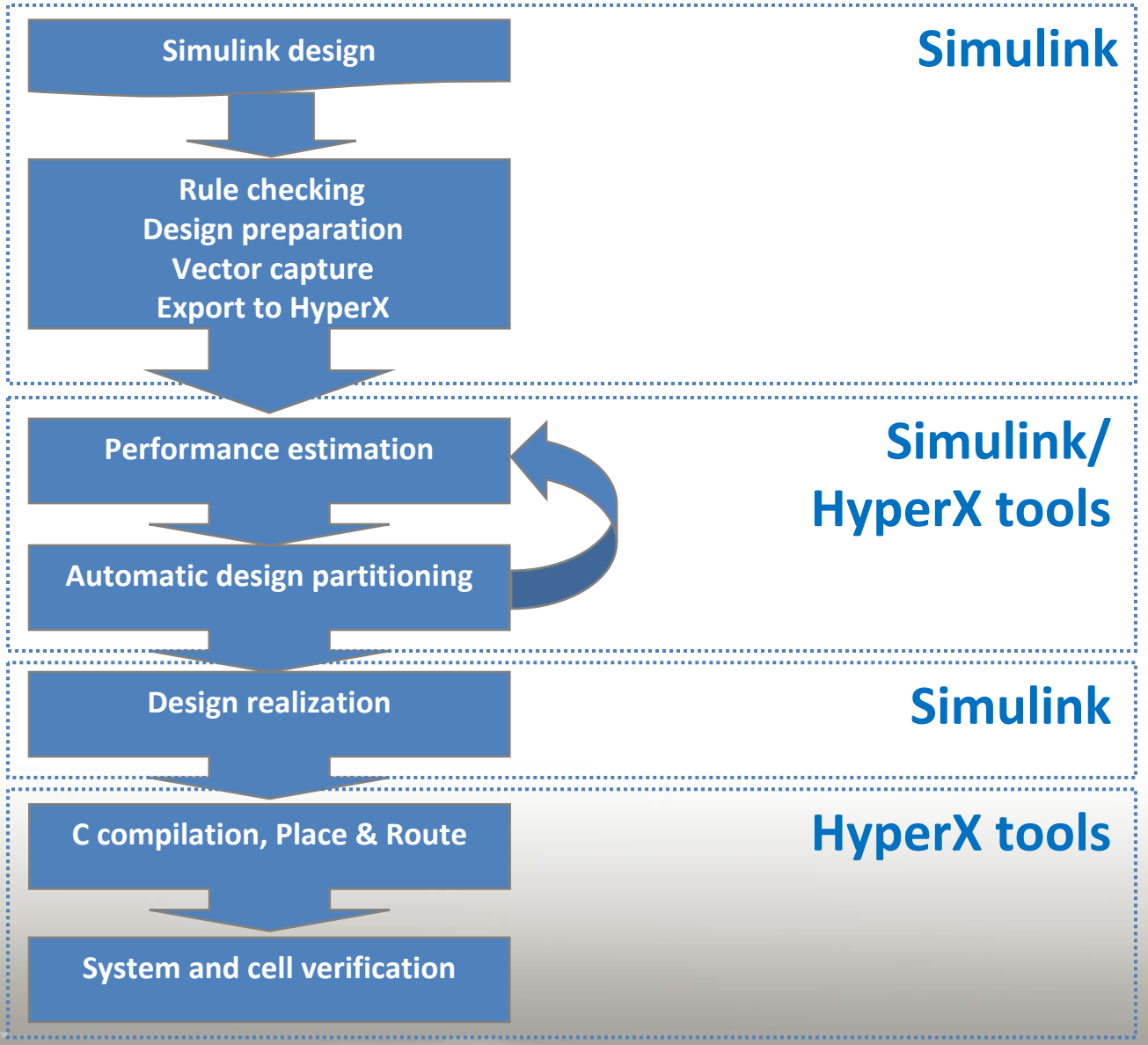
Waveform Application Development

Model Based Design Flow

Model Based Design Flow (MBDF)

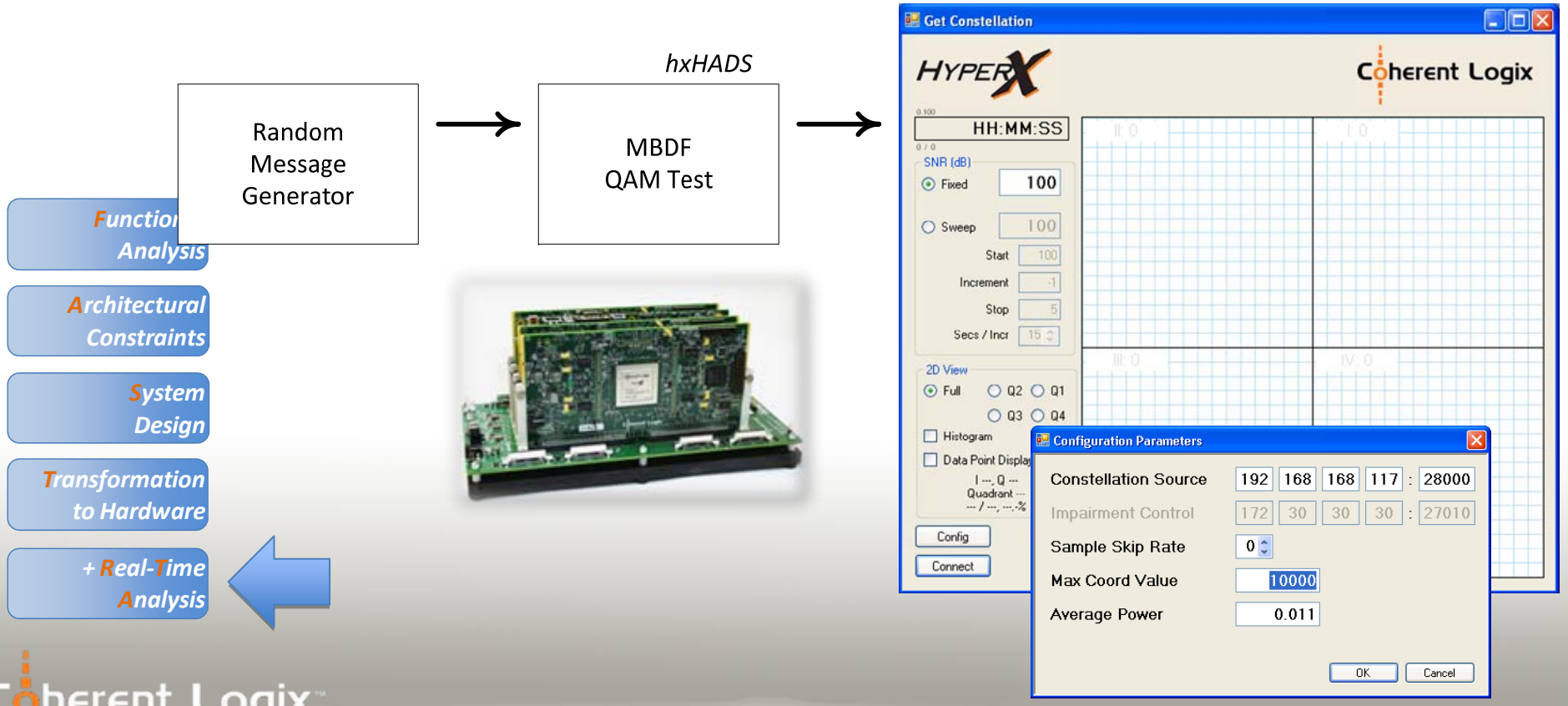
- **Fast design prototyping**
  - C-implementation extracted from Simulink flow given user supplied constraints
  - Leverages intrinsic block sets and code generation
  - Enables early design feedback regarding system throughput, link performance and resource utilization
- **Functional design verification**
  - Automatic test vector capture
  - Design and cell-based verification
- **Design optimization relative to initial flow**
  - Design re-/partitioning
  - Library cell replacement
  - Ongoing algorithm study/refinement

MBDF Overview

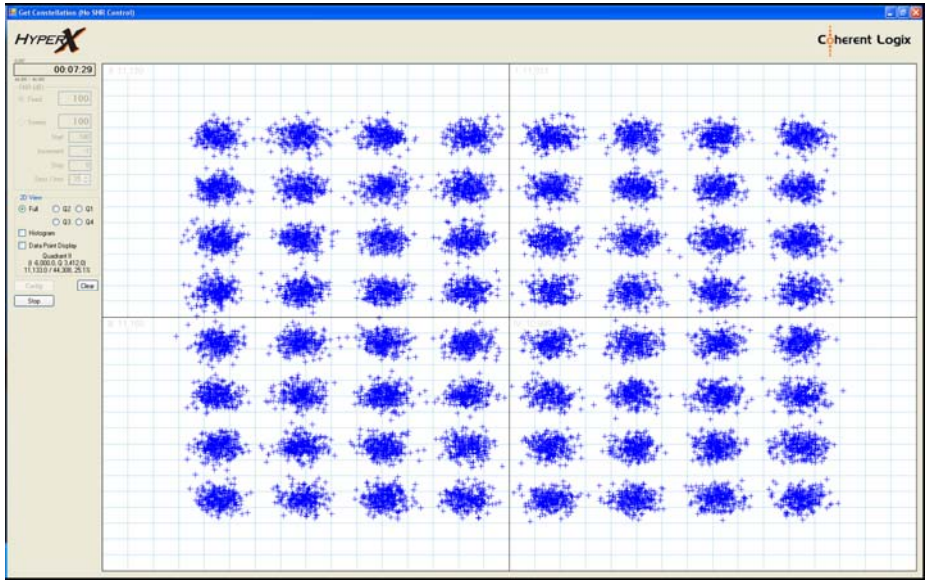


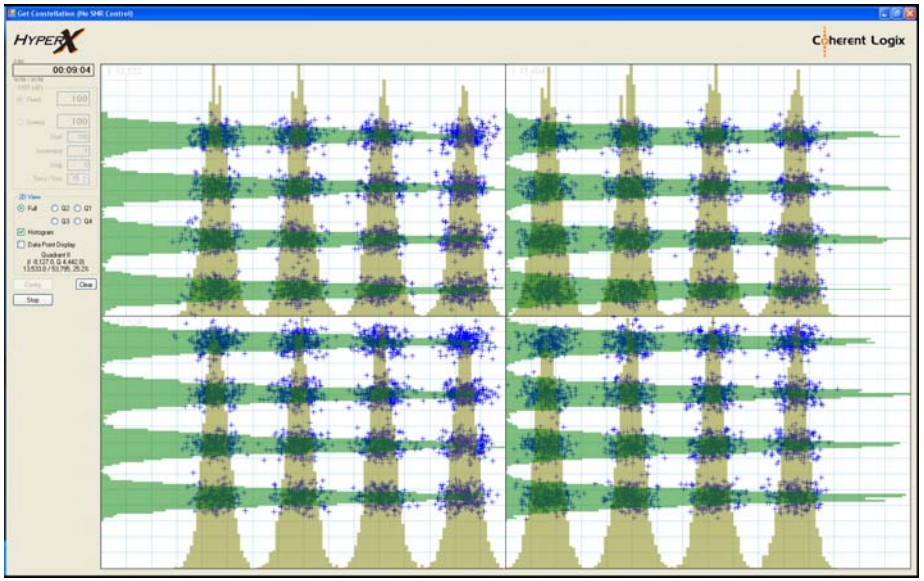
MBDF Example: QAM Modulation

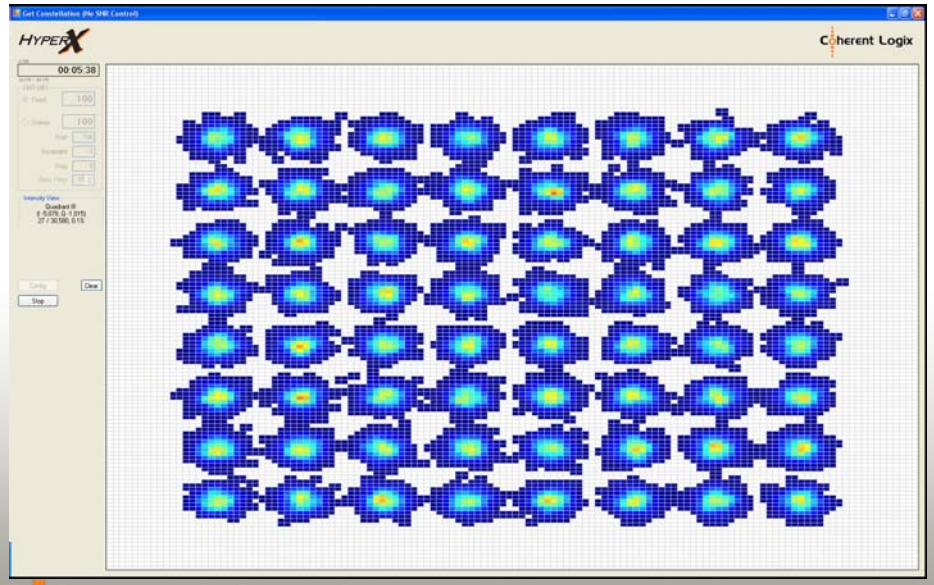
- **Automatically generated application targeting RWDS.**
  - Random message generator uses Tausworthe URNG.
  - Constellation display.

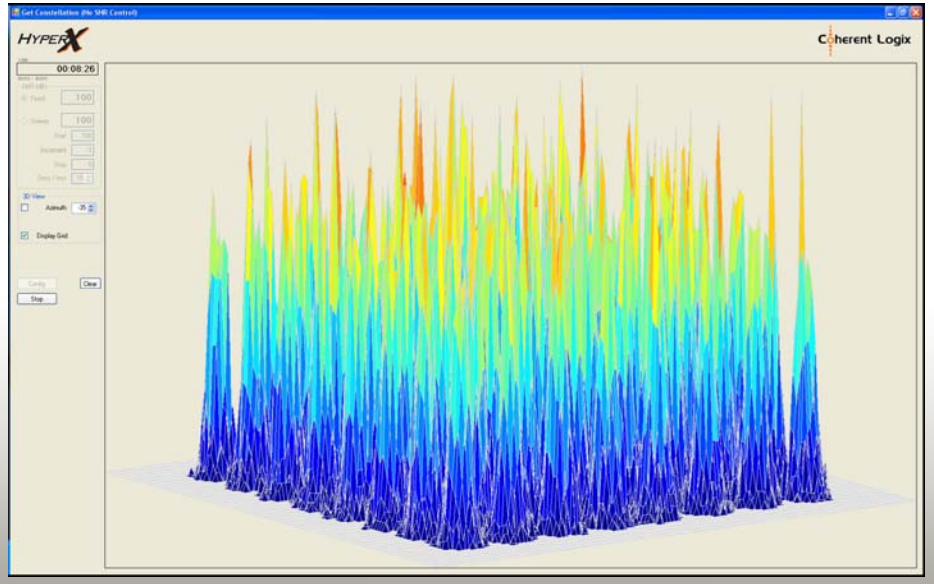


MBDF Example: QAM (64) in Real-Time – Constellation Display



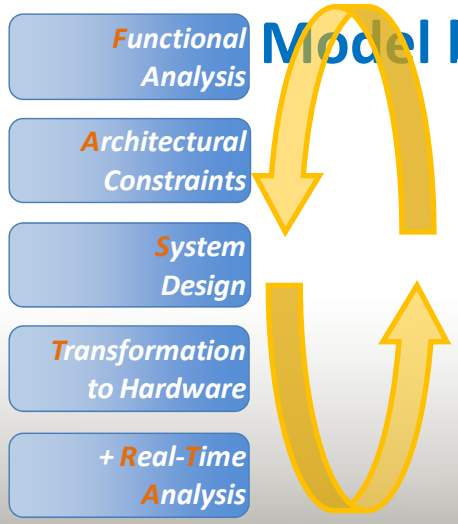


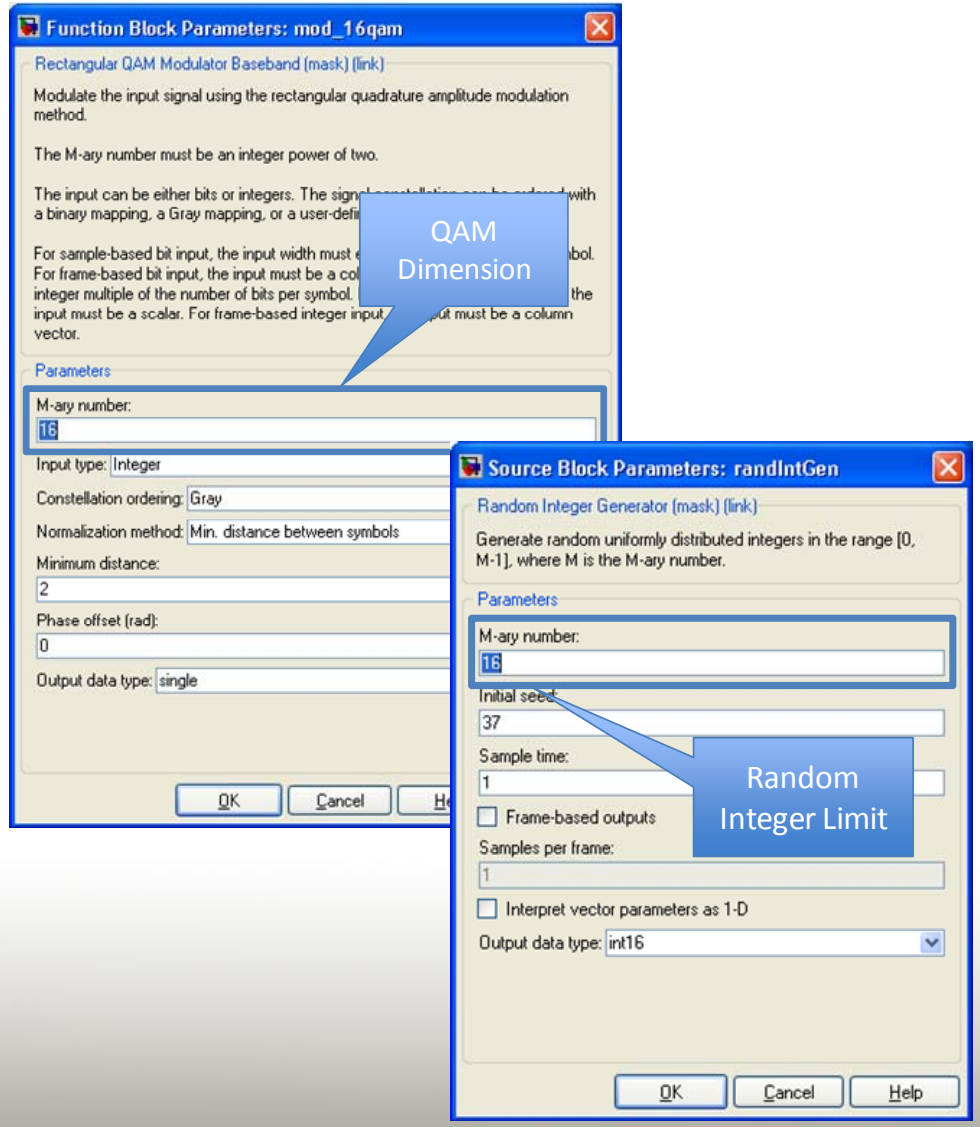




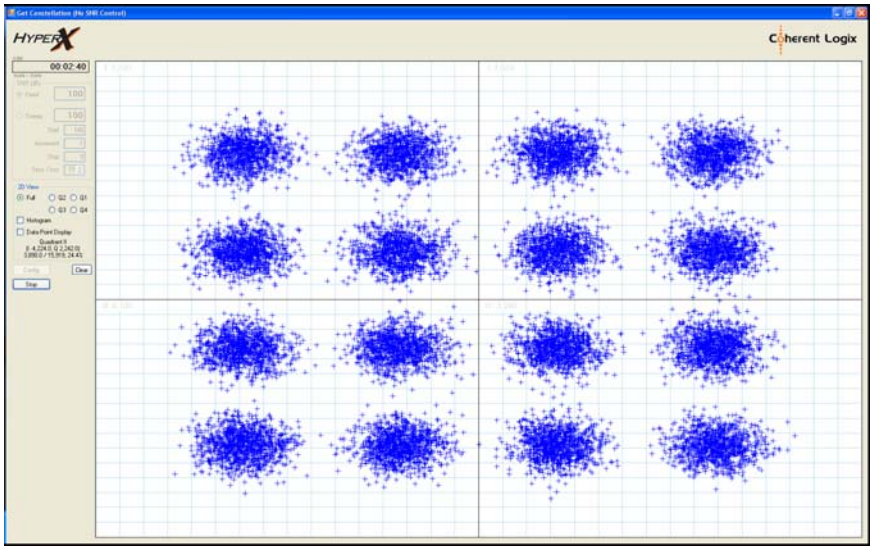
MBDF Example: 64→16-QAM

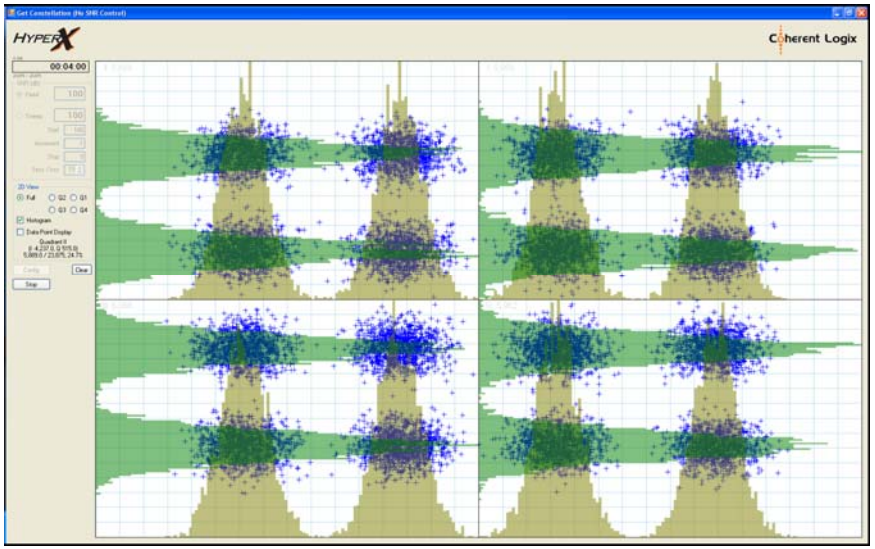
- **Design change at highest level of abstration**
  - Update single parameter on QAM module
  - corresponding change to random integer generator

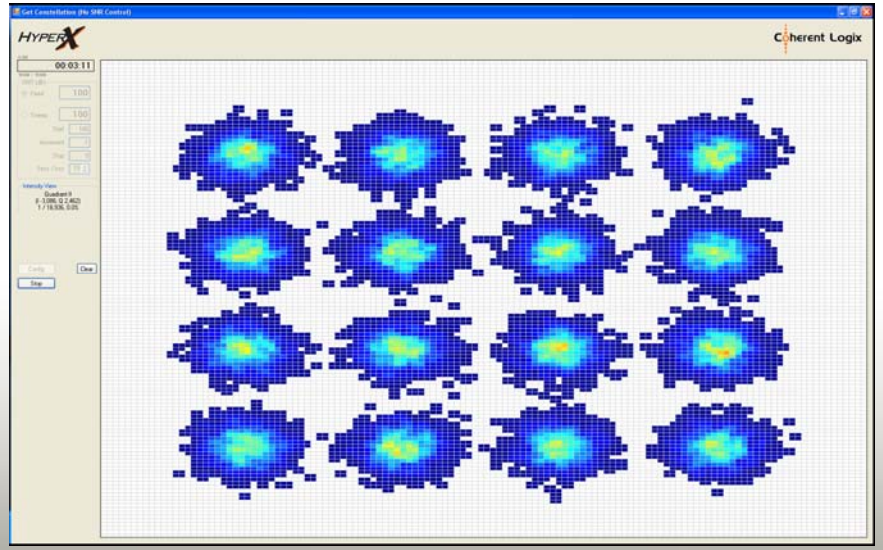


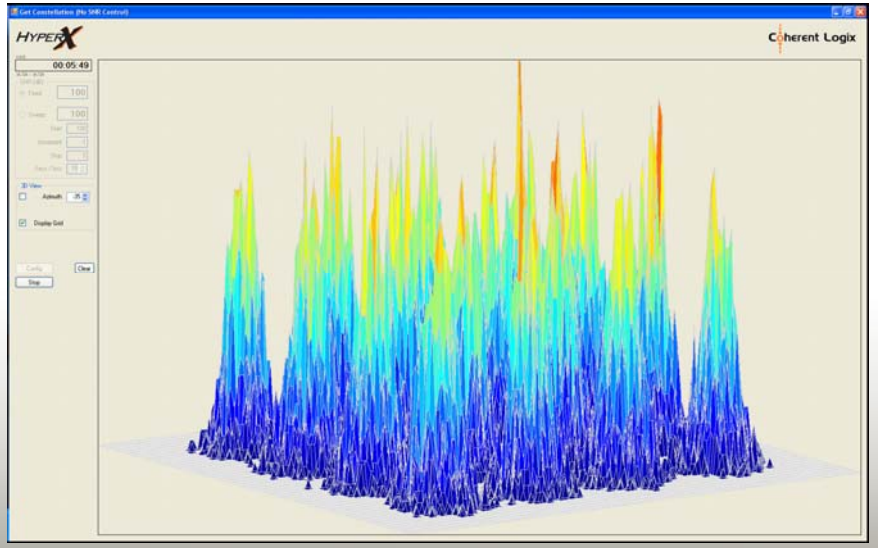


MBDF Example: 16-QAM Constellation Display









Waveform Application Development

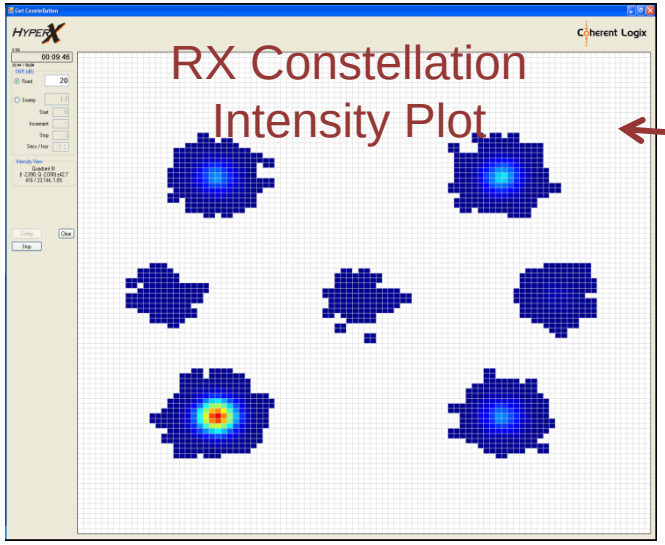
Real-Time Analysis

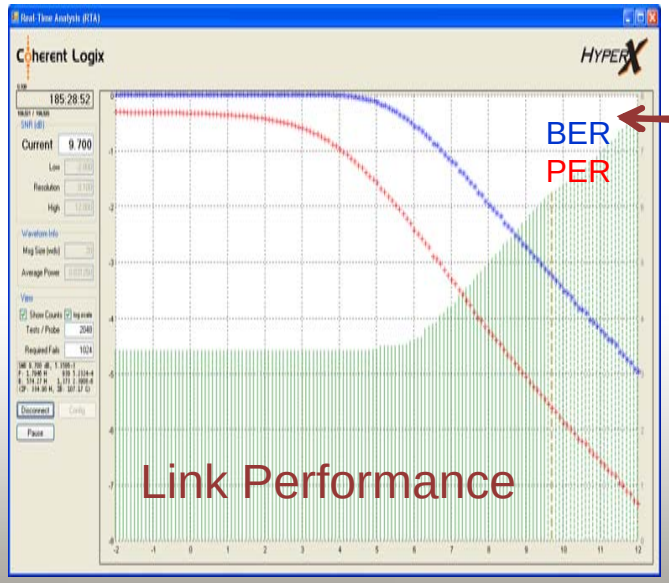
Real-Time Analysis

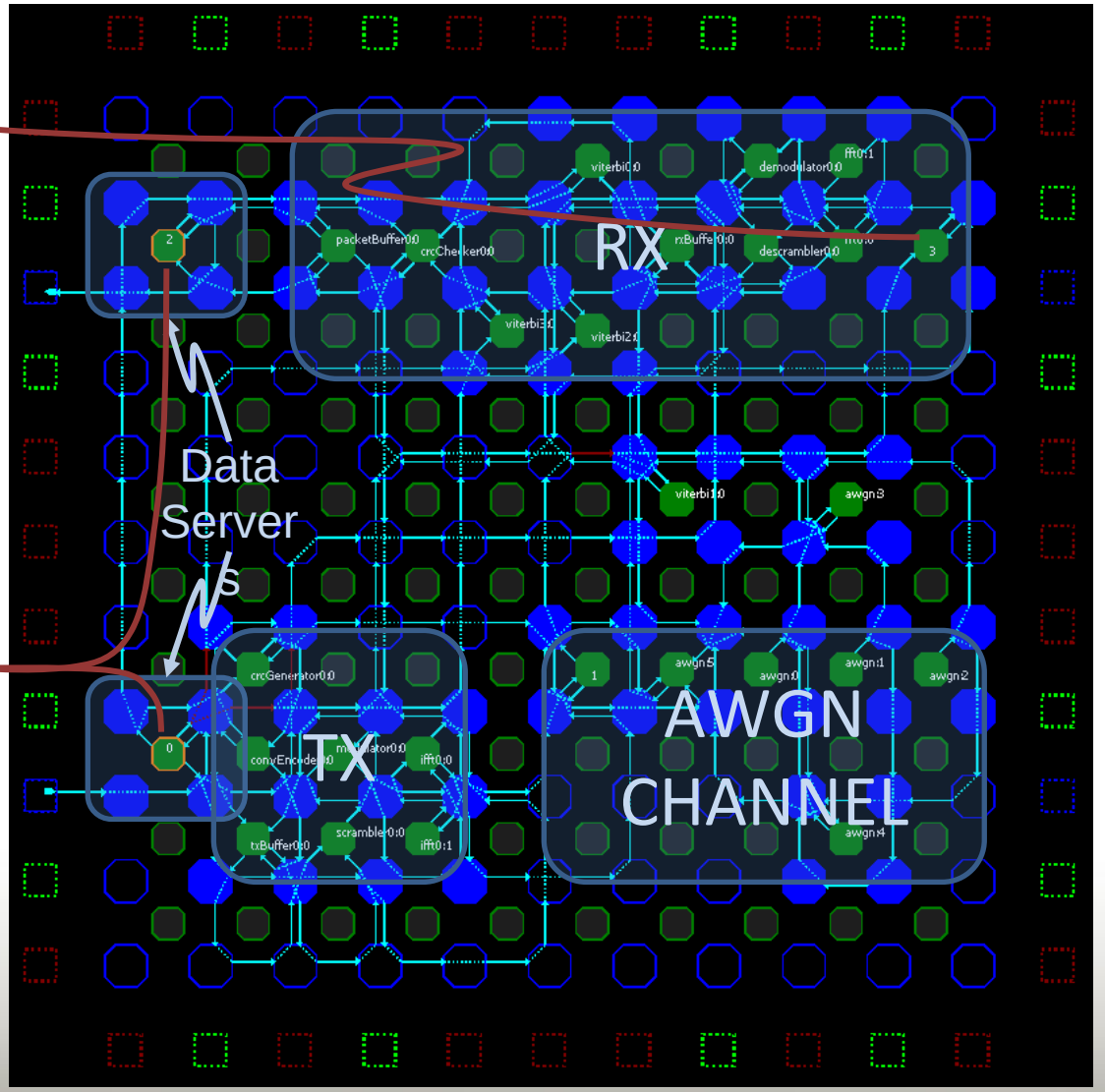
- **Takes design from highest available abstraction level to hardware, evaluating at each step**
- **Comprises:**
  - Run-time configurable Channel Impairments
  - Design Instrumentation
  - Link Analysis Tools
- **Enables:**
  - Real-time observability without perturbing system operation
  - Performance characterization throughout the waveform development process
    - Algorithm/Finite Precision tuning
    - Design Optimization: throughput, latency, resource utilization
    - Final waveform validation: BER/BLER, EVM performance assessment

⇒ **Productivity gains derived from real-time performance characterization and early design feedback**

RTA Example: BER / PER Characterization



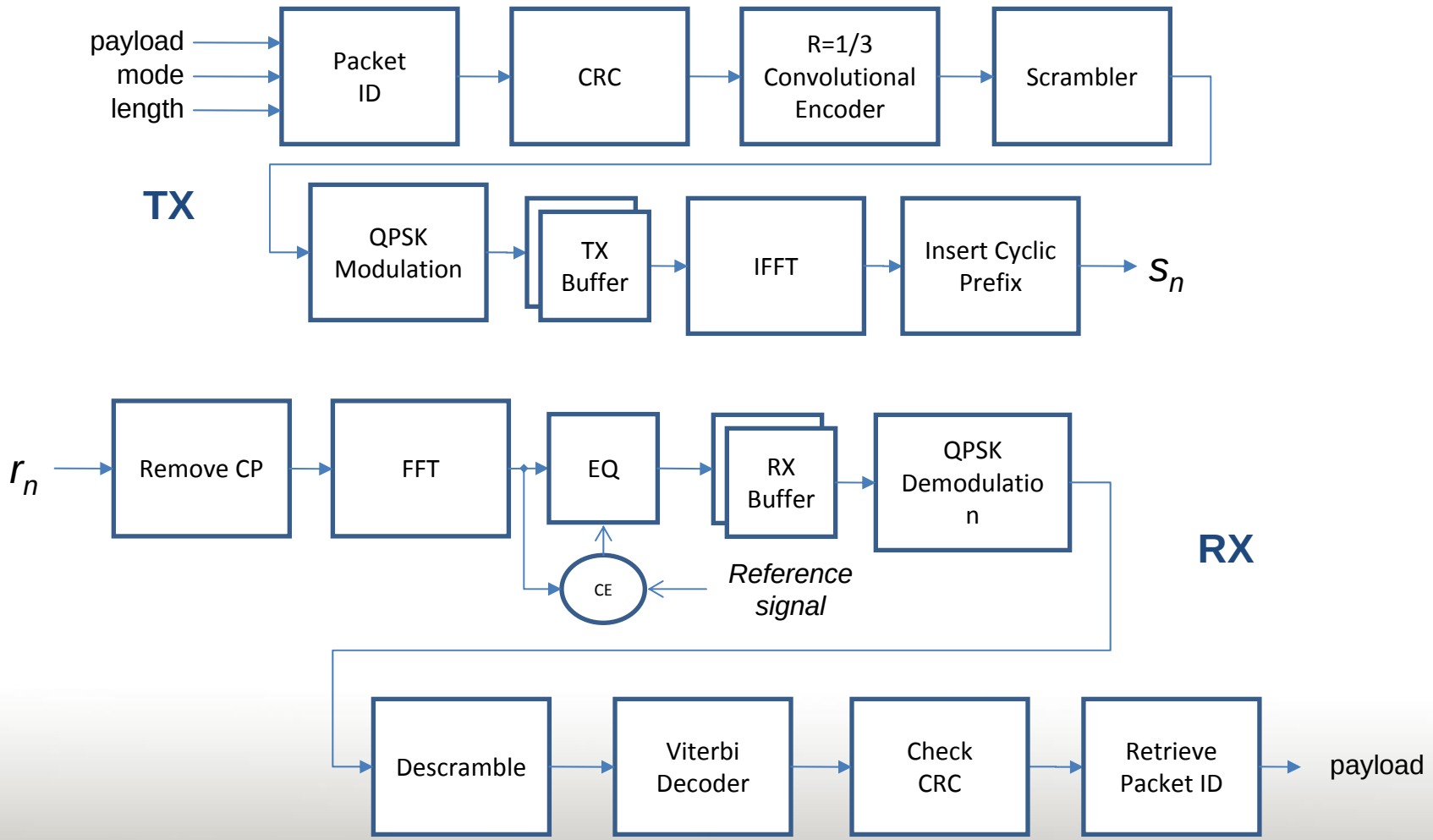




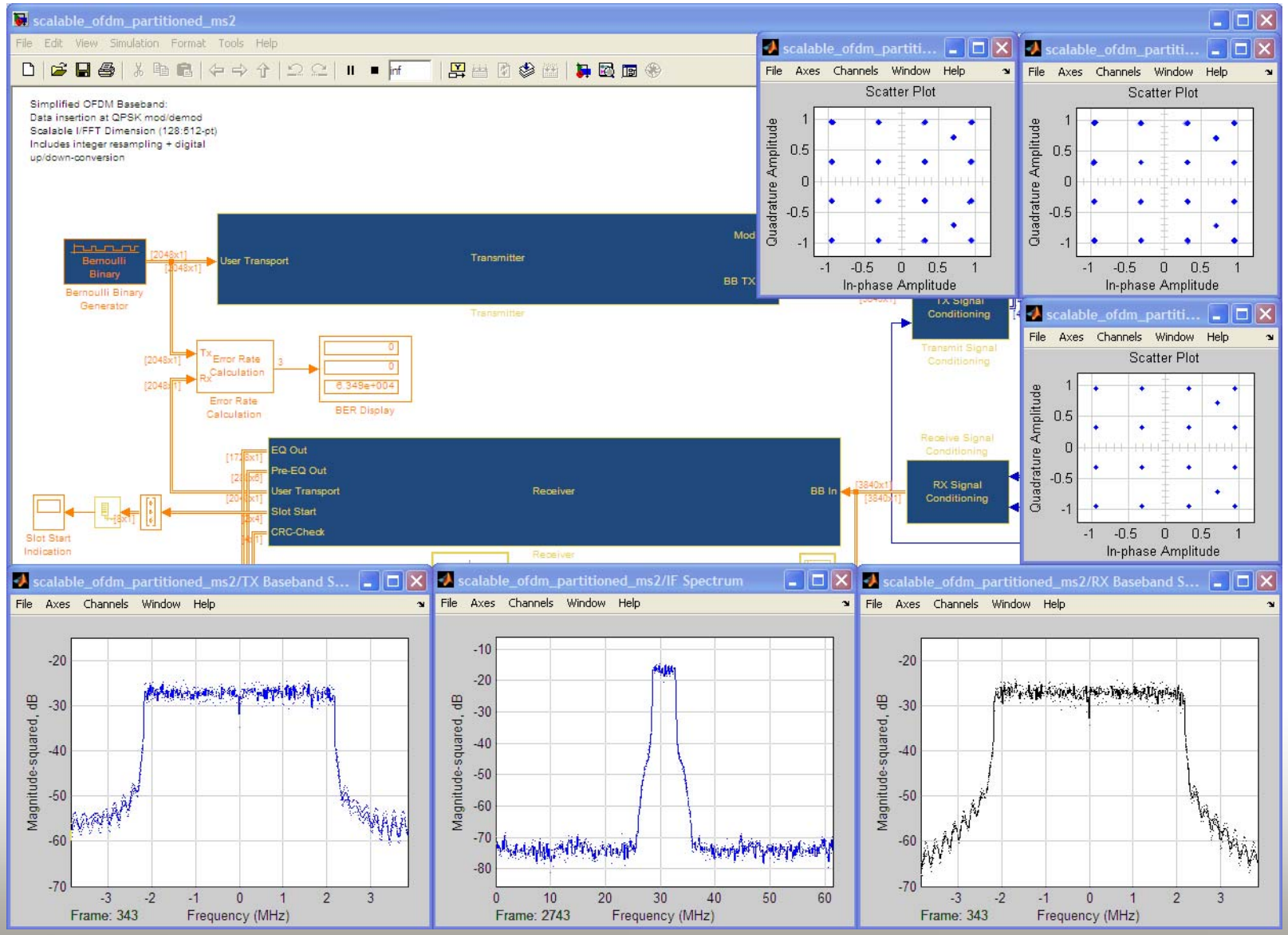
Reference Waveform Implementation

Scalable OFDM (SC-OFDM)

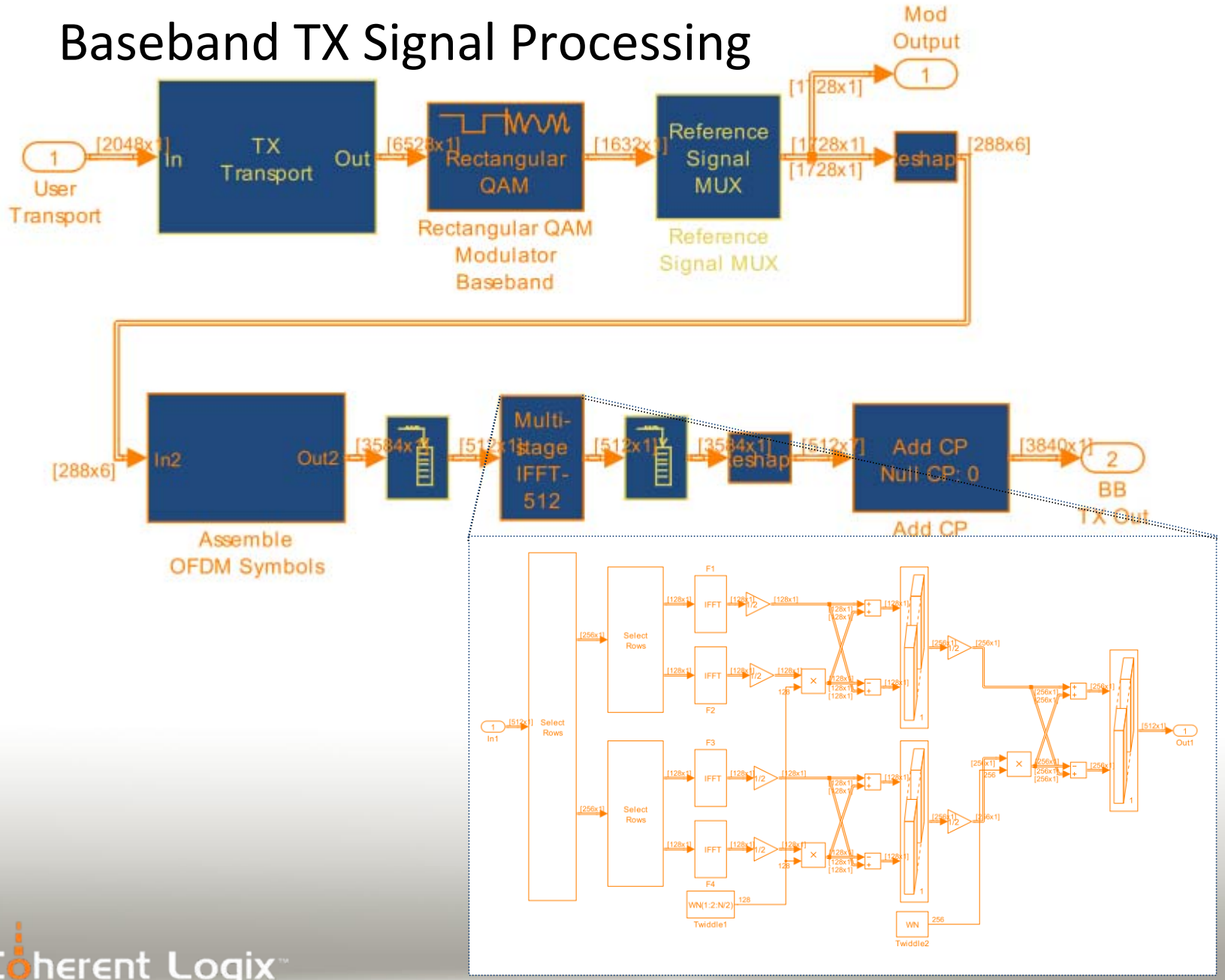
System Model



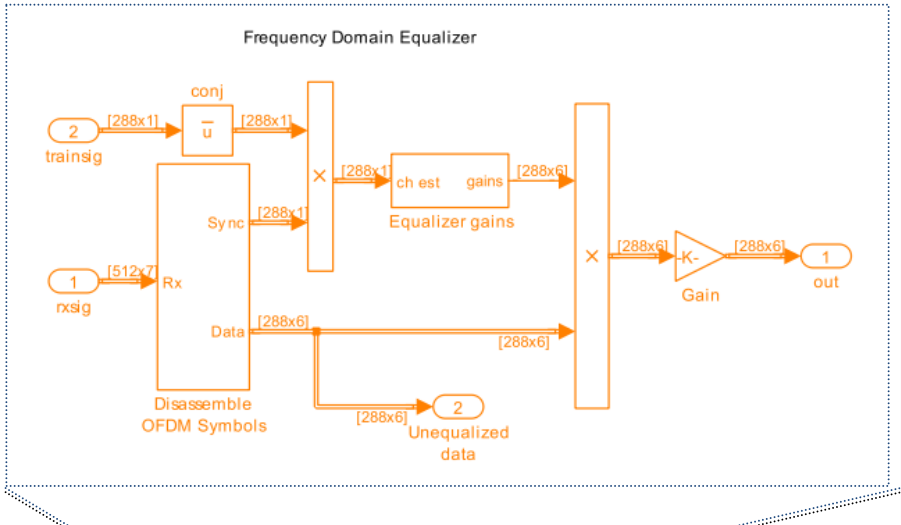
Simulink Model: 5MHz (512-pt I/FFT), 16-QAM

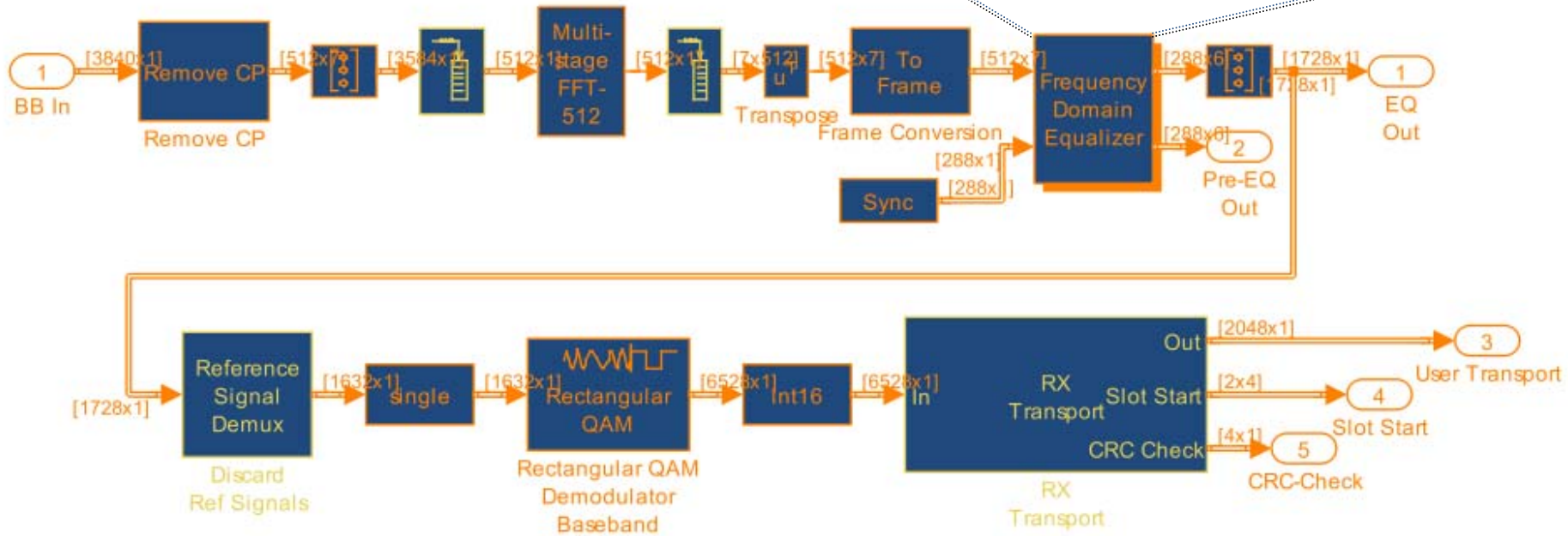


Baseband TX Signal Processing



Baseband RX Signal Processing





Transmitter Report

C:\CLX\workspace\WBDF_OFDM_Tx\clx_scalable_ofdm_partitioned_hw_Transmitter\pReport.txt - Notepad++

File Edit Search View Encoding Language Settings Macro Run TextFX Plugins Window ?

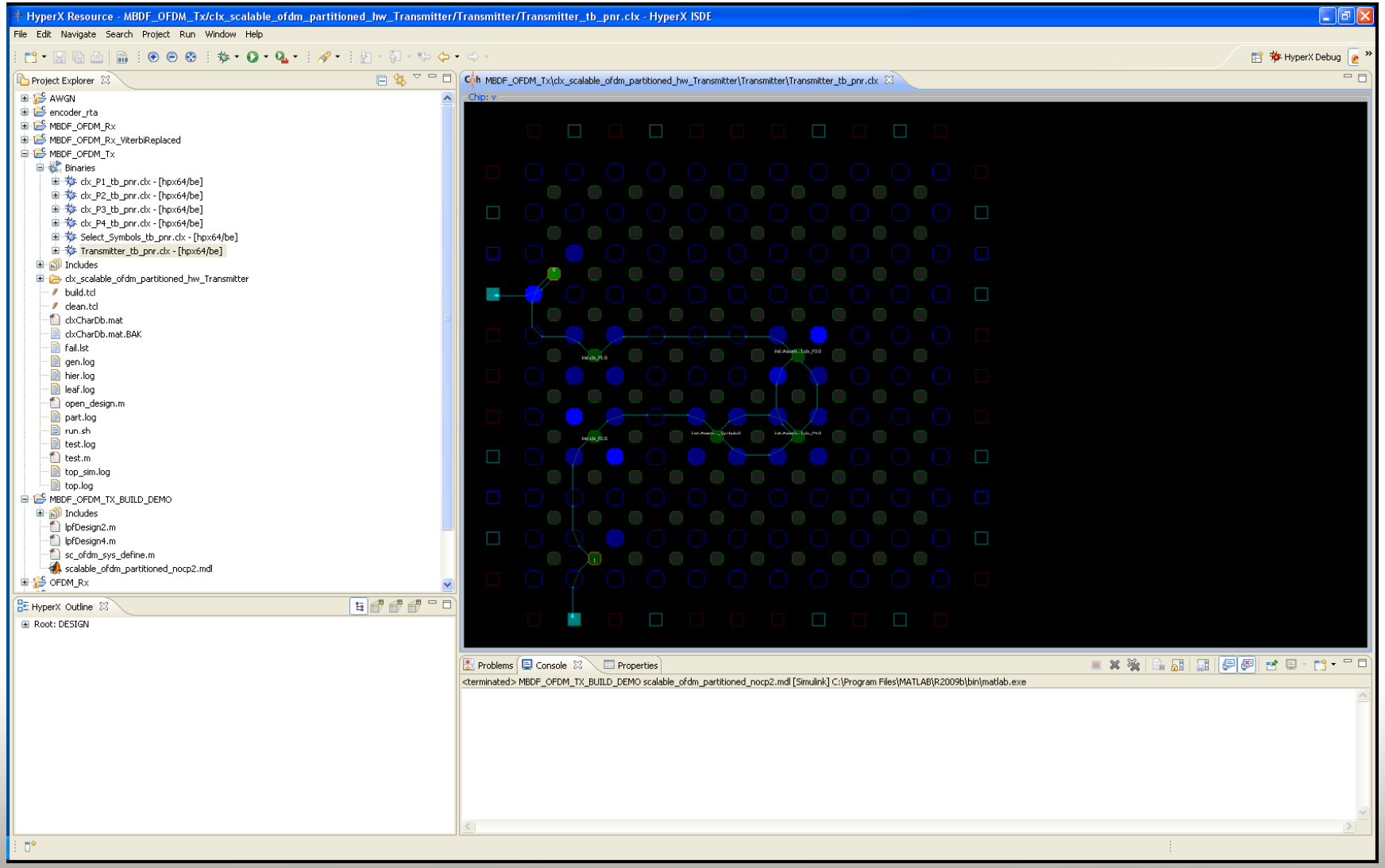
pReport.txt

```
1  Partition   Latency (cycles)     Code Size(words)     Data memory(words)
2  P1       207229           1392            7378
3  P2       230193           1595            14425
4  P3       1014             270          1756
5  P4       20445            1065            12930
6  P5       6894             474          4782
7
8  P1: IFFT_407_002(1), Reshape1(1)
9  P2: TX_Transport(1), Rectangular_QAM_(1), Referenc_202_001(1)
10 P3: Select_Symbols(1)
11 P4: Reshape3_191_001(1), DC_value(1), Assemble__k(1), Flip(1), Assemble_Subcarr(1), Pad1(1), Pad(1)
12 P5: DC_value1(1), Insert_Sync(1), Select__k__k_dat(1)
13
14 Total design throughput achieved: 230193
15 Total PE usage: 5
16
17 Design sample rate is 0.000500
18
```

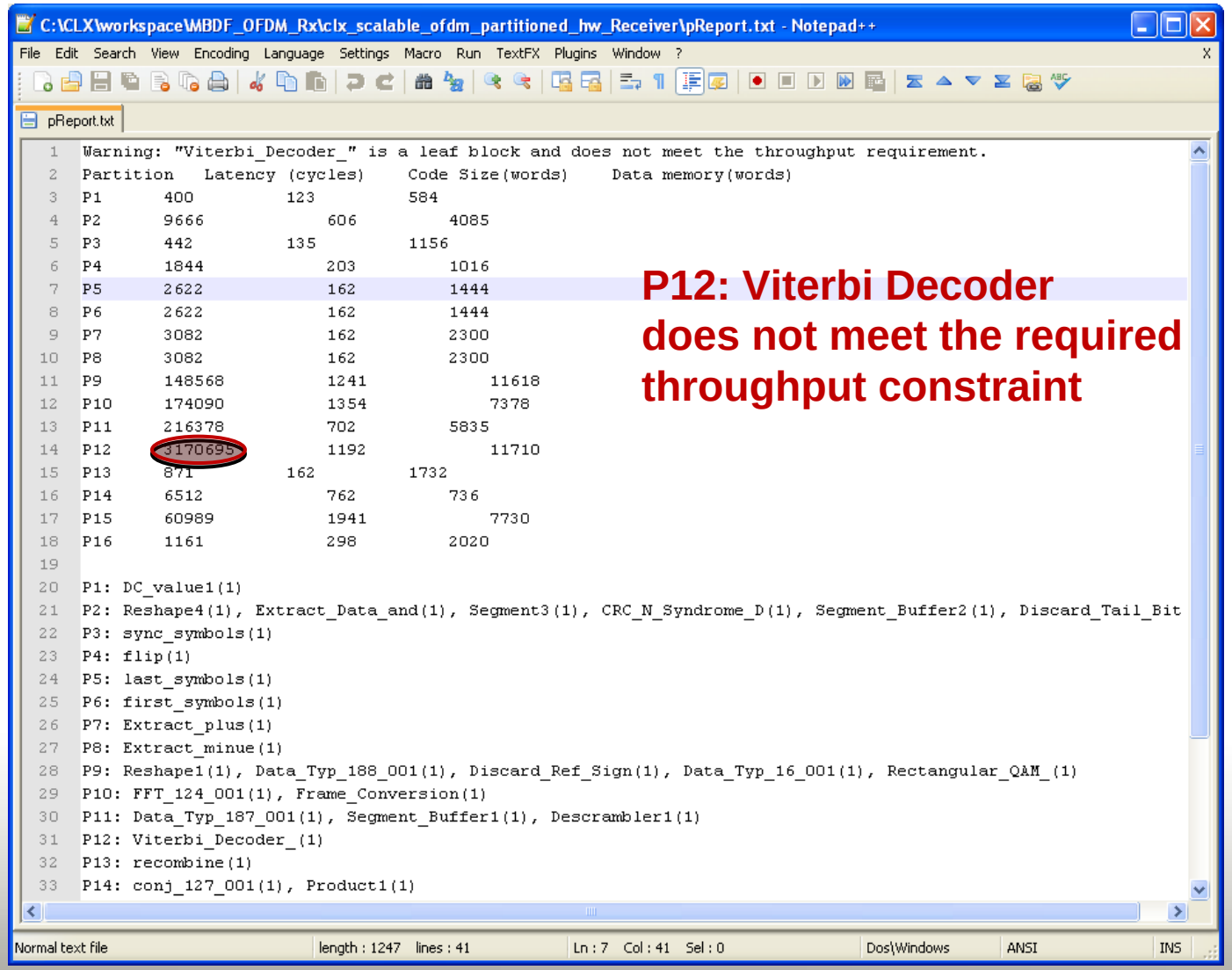
Normal text file | length : 564 lines : 18 | Ln : 1 Col : 1 Sel : 0 | Dos\Windows | ANSI | INS

All blocks meet 0.5ms throughput requirement
5 PEs

Transmitter Resource Mapping

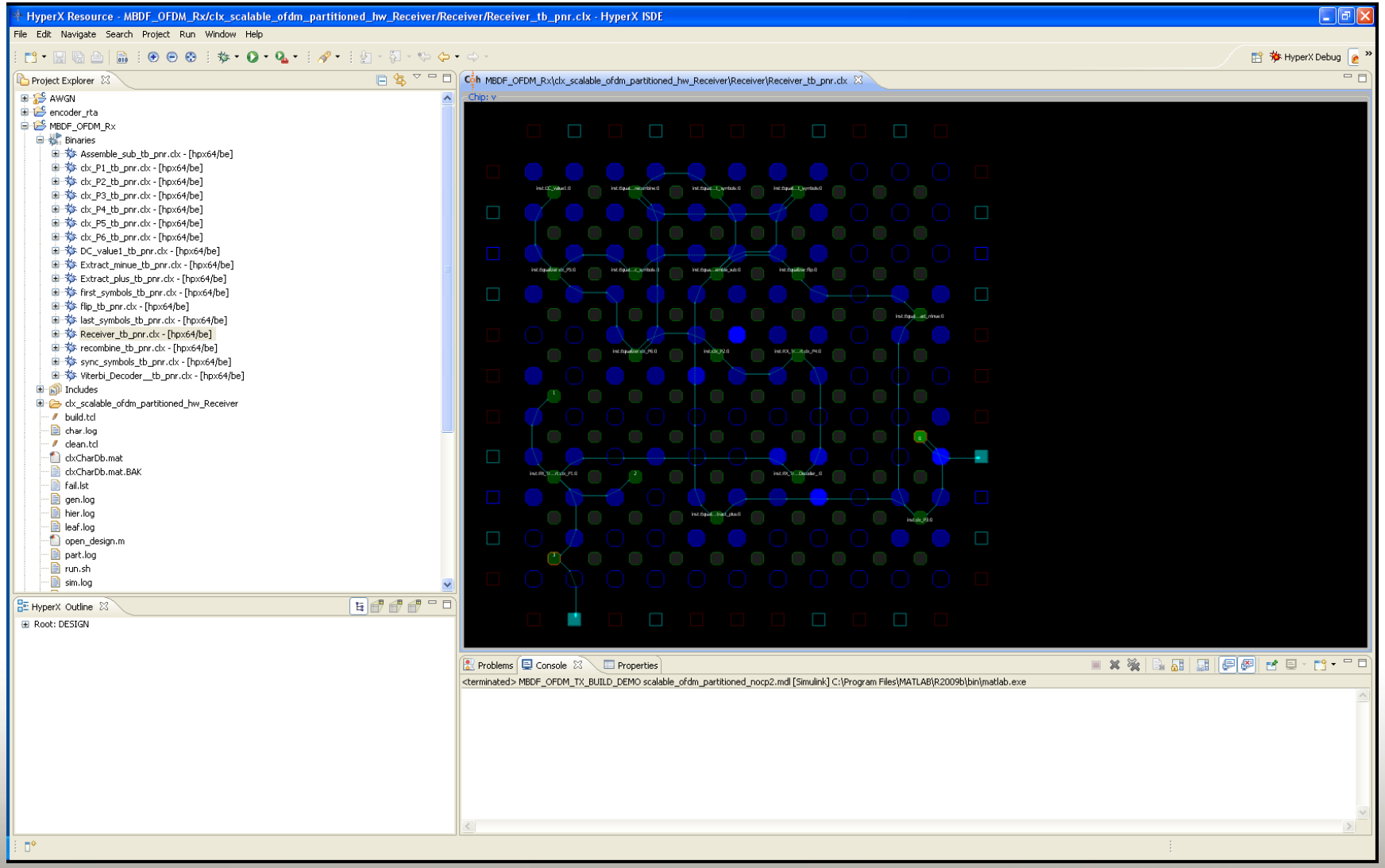


Receiver Report



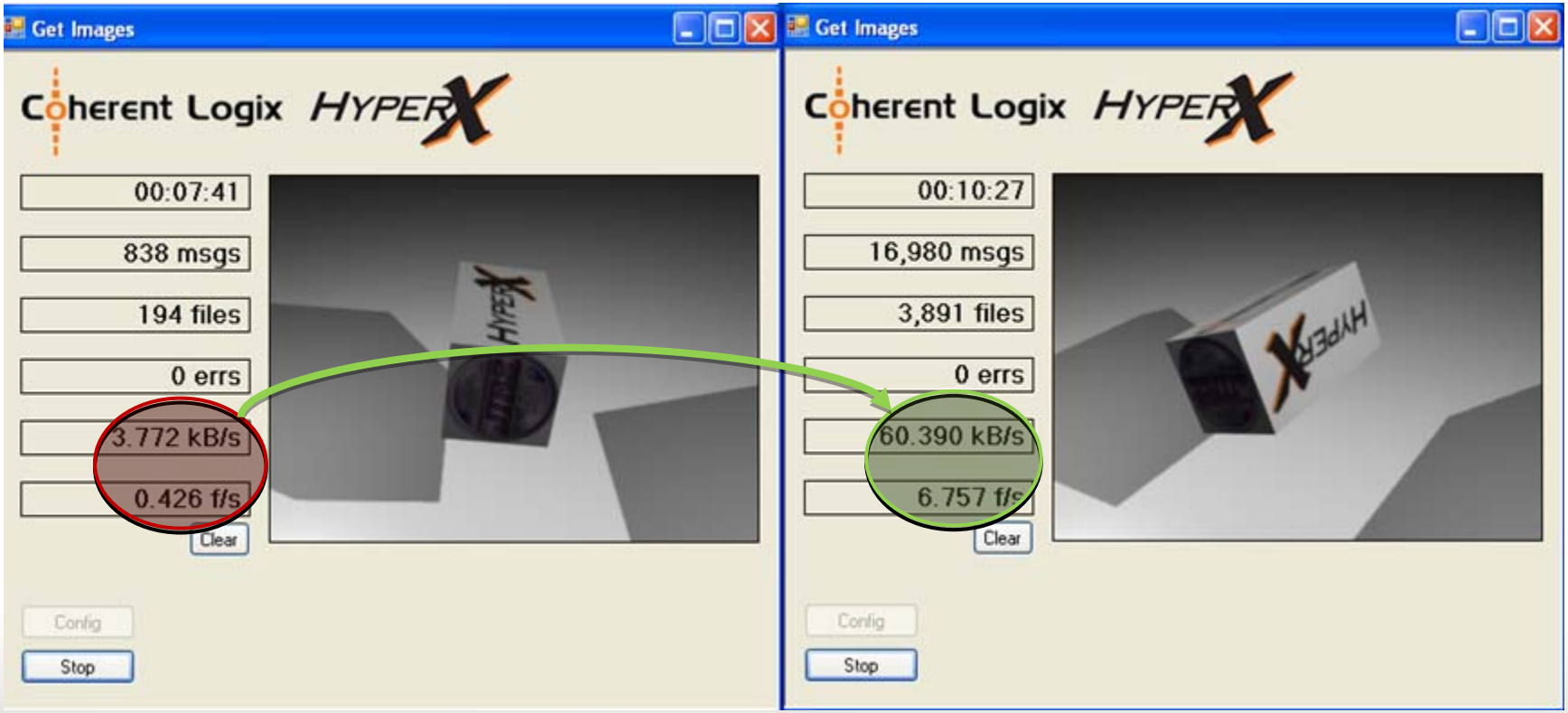
P12: Viterbi Decoder does not meet the required throughput constraint

Receiver Resource Mapping

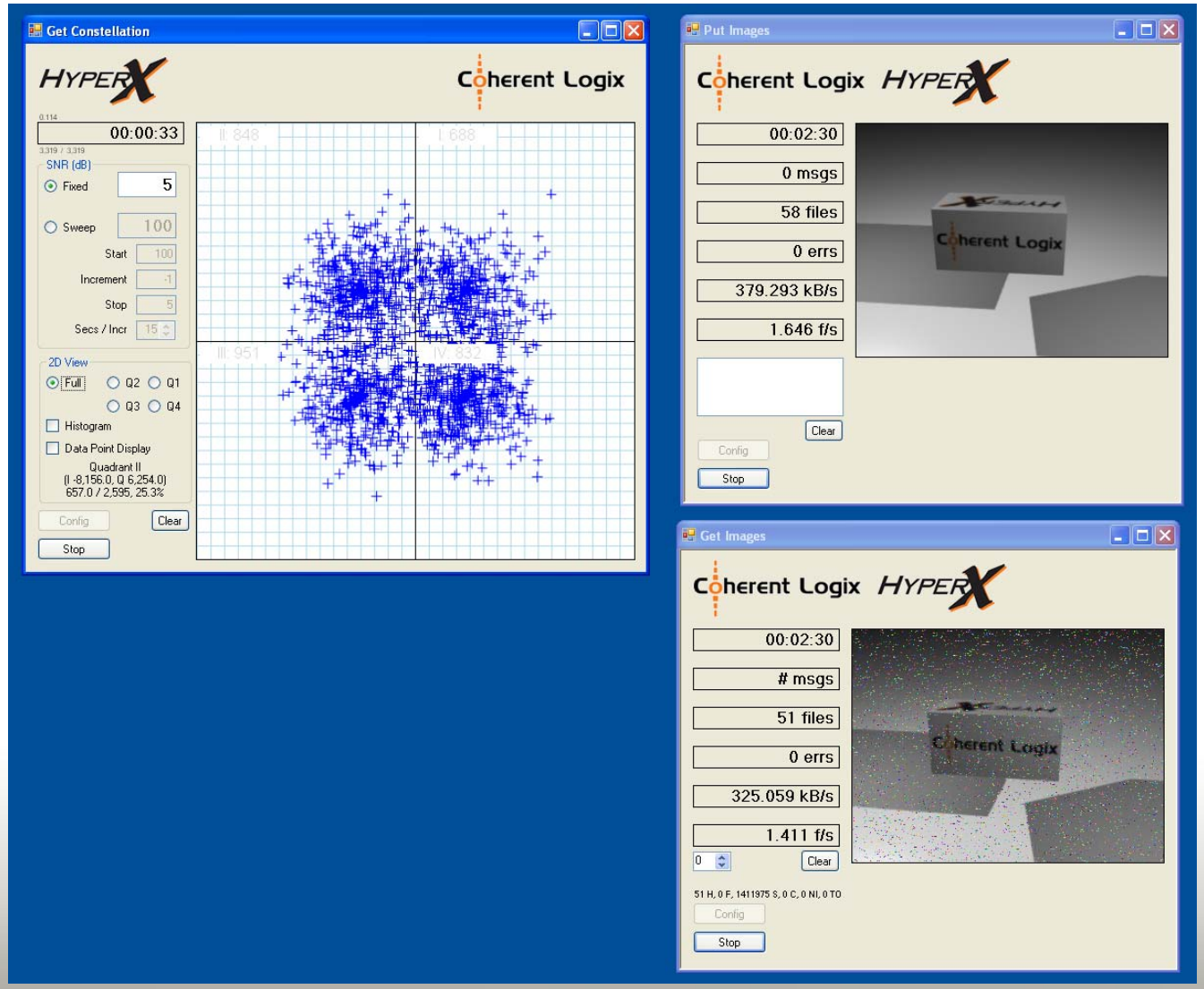


Cell Replacement – Viterbi Decoder

16X improvement in processing throughput via cell replacement



Hand Coded Design in AWGN



Closing Remarks

Conclusions and Ongoing Work

- **The RWDS**
  - Provides access to the HyperX signal processing complex in a real-time development environment;
  - Enables at speed waveform design and analysis from initial algorithm exploration through final implementation and performance characterization.
- **Provides seamless path to product form factor**
  - Migrates the signal processing chain through the data converter interface to a shared platform placed alongside the RF transceiver.
  - Preserves full software stack “as is”
  - Preserves hardware architecture, removing unnecessary glue logic
  - Provides real-time analysis, characterization, instrumentation, etc.

Q&A

Thank you for your time and attention!

Kevin A. Shelby, SDR Engineering Manager

Office of the Chief Technologist

Coherent Logix, Incorporated

Office: +1-512-382-8953, Fax: +1-512-382-8941

shelby@coherentlogix.com

Photo Courtesy NASA

Note

- **The latest version of this presentation and the corresponding paper will be accessible from the Coherent Logix, Inc. website after the conclusion of the conference.**

- **Please visit**

www.coherentlogix.com

for more details.