Ultra-Wideband 1.6 GHz Channelizer:
Versatile FPGA implementation

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Abstract

Increasing bandwidth demands and multi-platform communication standards require higher sample rates and call for highly parallel signal processing algorithms. This paper presents a proof-of-concept implementation of a 1.6 GHz channelizer implemented in a highly parallel processing platform. Although the implementation of signal processing algorithms was the design focus, dispelling common fears of handling digital I/O in the GHz range is an important contribution. Task specific devices designed for single standards (i.e. CDMA, GSM, OFDM) will not satisfy next generation system requirements. Versatility and reconfigurability to accommodate multiple standards will be a requirement to gain acceptance and future marketability. The need for software reconfigurability is particularly significant in the military communication arena. Recognizing that legacy and future modulation standards, bandwidths and carrier frequencies vary, this channelizer design provides the flexibility to meet requirements spanning a wide range of bandwidth and modulation formats. Higher sample rates increase system versatility at the expense of system complexity. Traditional DSP algorithms must be redesigned as parallel processes. The recently released Xilinx Virtex 4-SX (Signal Processing model) FPGA can efficiently implement complex parallel algorithms and mange the increased data rates, computing over 250 Giga/operations per second and terabit memory bandwidth. This proof-of-concept design demonstrates that the Virtex-4 FPGA can latch differential I/O rates up to 1 GHz. This design demonstrates how digital signals in the GHz range are cleanly managed by adhering to a few basic PCB routing rules, which should embolden designers to confidently tackle similar multi-Gigahertz digital designs.

Introduction

The multirate channelizer partitions and processes large input bandwidths by employing the computational efficiency of the polyphase filter and the Fast Fourier Transform (FFT) to simultaneously heterodyne, filter, and resample a single high-rate time series into multiple parallel channels.

Traditional Digital Signal Processing (DSP) channelizer solutions require a complex phase rotation followed by a FIR filter pair *per* channel, as shown in figure 1. Consequently, traditional M branch channelizer designs require M copies of the mixer-filter pairs. The FFT and the polyphase filter can more efficiently perform the operations of all M filter pairs by partitioning the input data stream to multiple low rate data paths prior to processing and then taking advantage of arithmetic redundancies to reduce the bandwidths to manageable blocks while processing at lower rates. Consequently, we compute the M = 32 path channelization with about the same resources required to isolate a *single* channel using traditional DSP techniques.
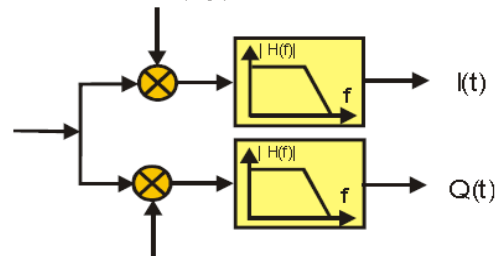

Figure 1. Complex phase rotators followed by filter pair.

When working with the channelizer we assume the entire sampled spectrum is occupied. The first step in our signal processing chain is to commutate and partition the input high sample rate time series to M, reduced-rate, time series. Here M is number of output channels. By forming multiple reduced-rate series prior to the bandwidth reduction, each new time series violates the Nyquist criteria and represents M-fold aliased data. The unique phase profiles of the M-fold aliases in each of the M-distinct paths permit the use of phase coherent processing to separate and extract any of the M-aliases.

The coherent processing can be partitioned into a set of *input* inner products over each reduced rate time series followed by an *output* phase spinning inner product over the sums so formed. The first inner products are seen to be a polyphase filter while the collection of output phase spinning inner products is a DFT, best performed by an M point FFT. The phase spinning sums destructively cancel all the aliases but the one alias selected to survive the sum. Thus the signal corruption, the aliasing caused by the input sample rate reduction, is removed by the post processing. The output of the channelizer's k-th channel is shown in (1). Here a low-pass prototype filter has been translated to the desired center frequency. This sum is partitioned into a double sum in anticipation of the up-

coming M-to-1 downsampling. In (2) we compute every M-th output sample and obtain the desired down sampled, by M, polyphase filter output. The downsampled output $y_r(nM)$ of the r-th branch is computed as a standard FIR filter convolution. If the original FIR 'h(n)' in figure 1 is of length 'N', then the length of each phase branch producing $y_r(nM)$ in (2) and seen in figure 2 as H_M is reduced by M to N/M coefficients operating at $1/M^{th}$ the input data rate.

$$y(n,k) = \sum_{\ell=0}^{N-1} x(\ell-n)\, h(\ell)\, e^{j\frac{2\pi}{M}k\ell}$$

$$= \sum_{r=0}^{M-1} \sum_{\ell=0}^{\frac{N}{M}-1} x(r+\ell M-n)\, h(r+\ell M)\, e^{j\frac{2\pi}{M}k(r+\ell M)} \quad (1)$$

$$= \sum_{r=0}^{M-1} e^{j\frac{2\pi}{M}kr} \sum_{\ell=0}^{\frac{N}{M}-1} x(r+\ell M-n)\, y(r+\ell M)$$

$$y(nM,k) =$$

$$\sum_{r=0}^{M-1} e^{j\frac{2\pi}{M}kr} \sum_{\ell=0}^{\frac{N}{M}-1} x(r+(\ell-n)M)\, h(r+\ell M)$$

$$\quad (2)$$

$$let\ y_r(nM) \doteq \sum_{\ell=0}^{\frac{N}{M}-1} x(r+(\ell-n)M)\, h(r+\ell M)$$

$$y(nM,k) = \sum_{r=0}^{M-1} y_r(nM)\, e^{j\frac{2\pi}{M}rk}$$

We see in (2), and in figure 3a, the set of phase rotators associated with the M-path polyphase filter. These rotators originally heterodyned the prototype filter to the desired center frequency and now extract the corresponding Nyquist band from the alias stack. The spectrum at the k-th Nyquist zone, aliased to base band by the M-to-1 re-sampling while preserving its unique phase profile related
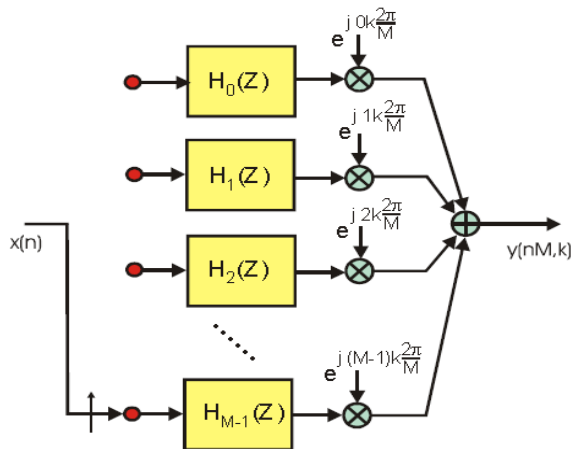

Figure 2. Polyphase filter bank and Complex Phase rotators to heterodyne the k–th Nyquist zone to baseband.

to its center frequency and time offset of the commutator process. These complex spinners align the phase profiles of each branch to extract the aliased signal from the k-th Nyquist zone by a constructive summation while canceling the other M-1 base band aliased channels by destructive cancellation. The spectrum of the k-th Nyquist zone is filtered and heterodyned (by aliasing), to baseband, as shown in the series of spectra in figure 3.
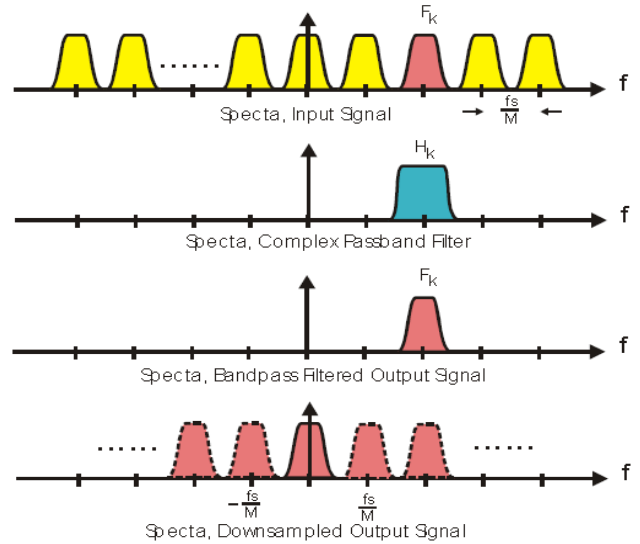

Figure 3. a: The Input Spectra and the k-th Nyquist zone (in red, F_k); b: Filter H_k; c: Isolated and filtered spectra of the k–th filter; d: Spectra of c now at baseband with spectral replicates at fs/M.

The effect of the phase rotated sum described in (2) and depicted as the process performed on the output of each filter branch of figure 2, can be interpreted as the output of one frequency bin of an M-point Discrete Fourier Transform (DFT). When multiple bins of the DFT are to be computed, the DFT is often implemented as a Fast Fourier Transform (FFT). The workload required to perform the M M-point phase rotations by the DFT and by the FFT are shown below.

$$DFT: M^2 \text{ Complex Multiplies and Adds}$$

$$FFT: \left(\frac{M}{2}\right) \log_2(M) \text{ Butterflies}$$

Perfect Multi-band Reconstruction

The versatility and efficiency of the polyphase channelizer can be further enhanced by additional post processing to construct a variety of unique *bandwidth /sample rate* profiles, using complimentary Perfect Reconstruction Filters (PRFs). The multi-band reconstruction of two or more channelized output signals to form a composite signal is equivalent to the functional inverse of the channelizer. The composite spectrum in general is wider than a single Nyquist channel. Similarly, a single transmitted

signal may be frequency division multiplexed (FDM) for encryption or other spectral considerations related to channel coding, and may need to be reconstructed from non-adjacent Nyquist zones.

When the desired spectrum is wider than a single channelizer bandwidth, several channels can be recombined to form a wider composite spectrum. Using standard filtering techniques, recombination of neighboring channels may lead to a composite filter response with undesired band edge boundary artifacts. Perfect reconstruction filters characteristically overlap spectra in a *perfectly* complimentary manner resulting in artifact free reconstruction.

As an example, figure 4b shows the spectrum of a real signal centered at 375 MHZ with a 150 MHz bandwidth. Figure 4a shows the frequency response of 4 (color-coded) complex channels of a 32 channel channelizer, each with 50 MHz bandwidth (with a 100 MHz sample rate) and centered at 300 350 400 450 MHz. The corresponding Nyquist zones are k = 6, 7, 8, and 9 of a 32 path polyphase filter, figure 8.

Of the 32 channels presented at the output of the FFT, four are represented and color coded in figure 4a. If viewed individually, each FFT output 'k' aliases the k-th channel to base band. Consequently all 32 Nyquist zones (or channels) collapse to DC, distinguished only by their unique phase profiles. Each must be heterodyned-up from DC to their proportional locations relative to the IF center of 375 MHz. The mathematical operations are:

1. Filter and heterodyne channel to DC, see (1).
2. Up-sample and interpolate to final data-rate.
3. Heterodyne (up) to appropriate frequency.
4. Repeat 1-to-3 for all required channels.
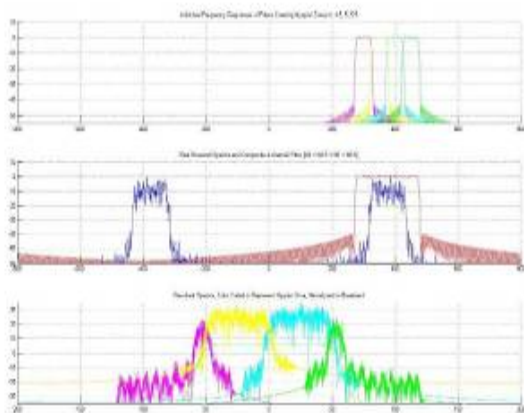5. Add all preprocessed channels.

Figure 4. A: Spectra of four Nyquist zones covering the band of interest; B: Input Spectra and composite filter; C: Color coded spectra at base band, perfectly reconstructed.

Steps 2-to-5 are efficiently handled using a smaller, inverted version of the 32-path channelizer as partially illustrated in figure 8. Figure 5 compares the direct baseband spectra and time series with the channel separated, down sampled, and up sampled and merged channelized process.
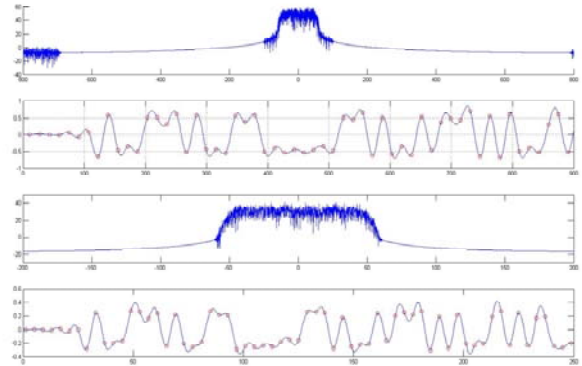

Figure 5. A: Spectrum of original 150 MHZ wide signal, at baseband, Fs = 1.6 GHz; B: corresponding time series; C: Spectrum of Polyphase Channelized, Downsampled and reconstructed signal, Fs = 400 MHz; D: Corresponding time series.

Features of Proposed System

By selecting the number of Nyquist zones needed to perfectly reconstruct a signal of interest, the sample rate must be adjusted in proportion to the bandwidth increase. Each Nyquist zone has a 50 MHz two-sided bandwidth with a sample rate of 100 MHz. Consequently, if four channels are combined, the bandwidth is 200 MHz with a 400 MHz sample rate. The composite sample rate is independent of the original carrier frequency and depends only on the signal's spectral width at the folding frequency. See figure 6, and [4].
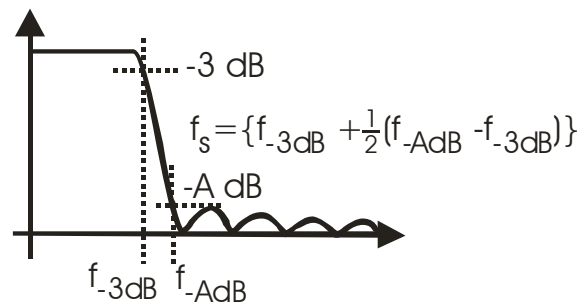

$$f_s = \{f_{-3dB} + \tfrac{1}{2}(f_{-AdB} - f_{-3dB})\}$$

Figure 6. Transition band determination points.

Direct IF-sampling

Because the bandwidth of the ADC (MAX108, Maxim Semiconductors) is 2.2 GHz with a sample rate of 1.6 GS/s, analog down-conversion is only required to the IF, thereby avoiding significant analog distortions caused by

I-Q mixer imbalances and filter frequency response mismatches. It is difficult to find I-Q mixer with imbalances less than 1 part in 100 and it is similarly difficult to maintain I-Q filters matching over time and temperature to the same tolerance. These two influences limit I-Q based image levels to approximately -40 dB.

Parallel Architecture

The high speed demands of a 1.6 GHz channelizer are efficiently satisfied using the Xilinx Virtex-4 SX version FPGA, which is a DSP specific FPGA, featuring 192-MAC engines operating at 500 MHZ (called a DSP48). The FPGA fabric can be viewed as a parallel computing engine, which provides a unique solution to the parallel processing required by this design. The 1.6 GHz input signal is quickly fanned-out to 16 synchronized and parallel paths, effectively reducing individual path-rates to 100 MHz. Furthermore, these 16 paths are perfectly structured as the 16-inputs needed by the 16-paths of the polyphase channelizer and subsequent 16-point FFT. A hardware resources utilization for the 16-channelizer design is summarized in table 1, for the Xilinx V4SX35:

Polyphase Channelizer	1200 Slices	32 DSP48s @400 MHz	
Streaming FFT	1600 Slices	32 DSP48s @400 MHz	32 BRAMS
Interpolating Filters	600 Slices	32 DSP48s @400 MHz	
Streaming IFFT	1000 Slices	8 DSP48s @400 MHz	8 BRAMS
TOTALS	4400/15360 = 29%	104/192 = 54%	40/192 = 21%

Table 1. Resource Utilization in Virtex 4 SX 35 FPGA.

Assessment and Comments

The theorized high speed task of bringing data into the FPGA at 1.6 GHz, i.e. 12.8 Gigabit /second has been proved in hardware and is completely operational. The high speed fan-out architecture is illustrated in figure 7. The Perfect reconstruction filters of the channelizer design cleanly reconstruct partitioned signals as can be seen in the time series representations of figure 5b and 5c. Further signal conditioning is accomplished via multi-channel equalization, which can be performed in hardware (FPGA fabric) or in software (soft-core) processor inside the FPGA. Channel dynamics may require hardware allocated to the equalization task equalization if the system is mobile and may only require software resources if the channel is static.
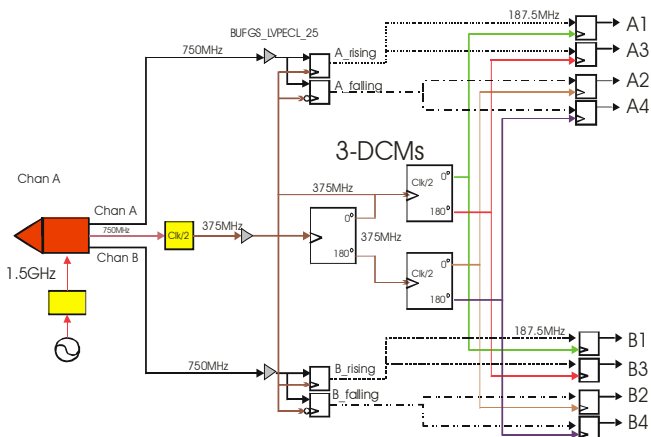

Figure 7. Parallel Architecture implemented and operational @ 12.8 Gigabit/Sec

Figure 8 shows the signal processing flow between the data collection point, the 1.6 GHz ADC and the final output of the 4-merged times series extracted from the 32-path polyphase filter and 32-pint FFT channelizer. Here we see the initial partition of the input data stream into 16 parallel input streams as 16 inputs delivered to the 32-path polyphase filter. The polyphase filter accommodates a 16-to-1 down sampling by performing a serpentine shift of the previous 16 input points into the next 16 addresses of the filter. The 32 output of the polyphase filter are passes to the 32 point FFT which operates at the 100 MHz data rate. In the example being described, the time series from 4-baseband channels are selected to be reconstructed as a wider bandwidth composite channel in an 8-point IFFT operating at the same 100 MHz. The FDM perfect reconstruction filter implemented in the 8-path polyphase filter completes the process.
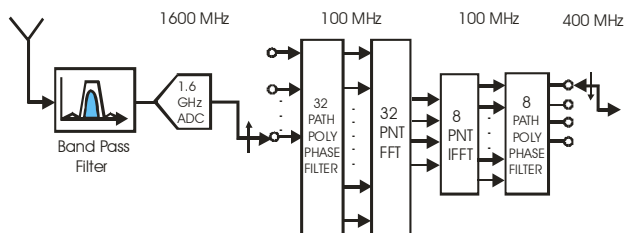

Figure 8. Signal Flow and Data Rate per section of the Channelizer and FDM Perfect Reconstruction Filter Bank

Figure 9 illustrates the mapping between the time series available from the output of the 32-point FFT and the spectral position of the channelized partition formed by the resampling polyphase filter and FFT phase rotator combination.
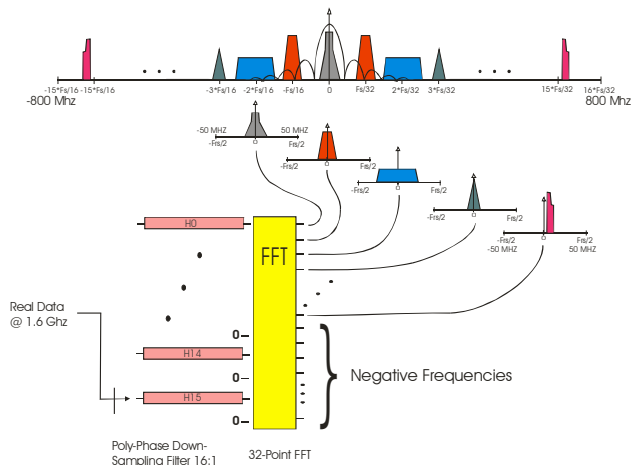

Figure 9. Representative illustration of channelizer, not completely accurate.

Conclusions

We have described the design and implementation of a high data rate channelizer implemented in a Virtex4 SX 35 FPGA. The sampled data time series processed by the channelizer is collected and formed in a Maxim MAX108 ADC operating at 1.6 GHz. Detailed information on the development board on which the design was implemented and tested may be obtained from the authors and may be found on Xilinx's web page.

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