AN ALL DIGITAL QAM MODULATOR WITH RADIO FREQUENCY OUTPUT

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ABSTRACT

A software defined radio (SDR) terminal promotes programmable realizations of the physical layer functionalities. A lot of research work has been done in applying digital signal processors (DSP) and field programmable gate arrays (FPGA) to implement the baseband functionalities of the physical layer. In this paper, the programmable solutions are extended to the radio frequency (RF) band for the transmitter. Digital pulse width modulation (PWM) technique is used to generate binary signals at radio frequency. A QAM modulator, combined with PWM, is implemented using off the shelf FPGA. The output of this all digital transmitter has a center frequency of 800 MHz.

1. INTRODUCTION

A software defined radio (SDR) is defined as a radio in which the digitization is performed at some stage downstream from the antenna. Then the radio can use flexible and reconfigurable functional blocks for the implementation of digital signal processing algorithms. As technology advances, the digitization might be at, or very close to the antenna, such that almost all the radio functionalities are realized using software using high speed and reprogrammable digital signal processing engine [1].

The current radios consist of a mixture of analog and digital building blocks. The radio frequency (RF) functionalities are most likely being implemented using analog circuits, while the baseband functionalities are more suitable for DSP implementations. Digital front end (DFE) is often used to bridge between radio frequency and baseband processing [1]. The DFEs are normally capable of processing signals with frequencies at about tens of mega-hertz, often referred to as digital intermediate frequencies (IF). Therefore, there remain significant analog blocks between the RF and digital IF.

Digital RF transceivers are studied to extend the software defined functionalities into the radio frequencies [1]. The focus of this paper is about all digital transmitter technology. The advantages of all digital transmitters are:

- high efficiency power amplification ([2], [3])
- digital combining of signals from multiple channels
- software programmable, or reconfigurable

Using an all digital transmitter, the entire transmitter can be realized using DSP or FPGA, which can take advantage of the rapid performance increase of CMOS technology. Besides its compatibility with SDR's requirement, DSP based RF system can also be made to compensate for the impairments of the RF channel. Therefore digital generation of signals directly at radio frequency has drawn a lot of interests among researchers and engineers.

One of the more traditional methods is described in [3], which uses band-pass delta-sigma modulation to generate binary signals at radio frequency. Binary signaling can be used together with switch mode power amplifiers (PA) to achieve higher efficiency comparing to other types PA technology. This transmitter architecture is shown in Figure 1. The drawback of this architecture is that the band-pass delta-sigma (BPDS) modulator is running at 4 times of the center frequency, which can be several giga-hertz. In order to accommodate such high frequency of operations, custom integrated circuits have to be very carefully designed, which lacks re-programmability.

Another method uses pulse width modulation (PWM) [4] to synthesize binary RF signals digitally. PWM was introduced as an analog modulation long time ago, but has gained popularity recently, especially in the digital audio amplification applications. Class-D audio PA, driven by PWM modulated audio signals, can achieve efficiency above 90%. Delta-sigma type of modulation can also be used in digital PWM, but operates at much lower frequency compared with aforementioned BPDS method. However the delta-sigma loop tends to be more complicated than what is used in BPDS, because of the low over-sampling ratio and the non-linearity associated with PWM.

Both references [3] and [4] only presented simulation and non real-time test results. The test setup uses signal sources computed offline that are stored in pattern generator. In this paper, a real-time system was designed to demonstrate the capabilities of digital generation of RF

signals using digital PWM. The rest of this paper will be organized as following. First, the method of generation of binary RF signals is discussed. Next, the different noise shaping behaviors between PWM and traditional DAC are described. This difference will lead to the discussion on our noise-shaping filter design method for the digital RFPWM system. Then the detailed implementation of an all digital transmitter based on digital RFPWM is presented. The final section summarizes the paper and presents conclusions.

2. DIGITAL RFPWM GENERATION

2.1. Digital PWM

Digital pulse width modulation (PWM) was motivated by the digital power amplification technique, by which a digital signal can be converted directly into high power analog signals without intermediate digital to analog converter (DAC) stages [5]. The digital power amplification has gained some popularity in the digital audio applications, due to the increasing interest to develop all digital audio system. In digital PWM, the pulse widths are quantized with respect to a high speed clock. Therefore a simple counter can be used to generate the digital PWM waveform based on the reference high speed clock. The general signal processing blocks consist of a digital PWM system are shown in Figure 2:

- Interpolator. The interpolator increases the sampling frequency of the PCM input to a frequency suitable for performing PWM modulation. In this paper, this frequency is referred to as pulse repetition frequency (PRF).
- Natural Sampler. The natural sampler calculates the naturally sampled signal values based on the uniformly sampled digital signal. It has been shown that naturally sampled signal experiences far less baseband distortion comparing to uniformly sampled signal, when PWM is performed [6].
- Quantization with noise shaping. The quantization is necessary to make the high speed reference clock running at reasonable frequencies for implementation purpose. For example, if the original PCM input is 44.1 KHz, a 16 times interpolator will result in the PRF equals to 705.6 KHz. The high speed reference clock needs to have the frequency of 46 GHz if the pulse width is quantized to 16 bits. If only 8 bits are needed to quantize the pulse width, the frequency of the high speed reference clock can be reduced to 180 MHz, therefore makes it much easier to implement using moderate technology. Noise shaping technique, e.g., delta-sigma modulation, can be used to suppress the baseband noise introduced by quantization.

One can also see that the processing intensive blocks, natural sampler and quantization with noise shaping, have the sampling frequency of PRF. This is the main motivation of this work: the main signal processing algorithms are executed at the lower PRF rather than the RF. In order to accommodate the bandwidth requirement in the QAM modulator in our demonstration, this difference is 100 MHz versus several GHz.

2.2. All Digital RFPWM

The method of an all digital radio frequency pulse width modulation RFPWM was introduced in [4], called quadrature integral noise shaping (INS). INS is an algorithm used in the quantization and noise shaping block. Its main goal is to suppress the noise power in the baseband introduced by the pulse width quantization process. It differs from other algorithm by introducing non-linear terms into the feedback loop. The details of INS are provided in [7]. Without considering the details of the INS algorithm, the quadrature INS can be viewed as two individual PWM modulators for inphase (I) and quadrature (Q) paths of complex signals respectively. These PWM modulations use the same architecture as described in subsection 2.1. The outputs from these PWM are baseband signals that need to be further mixed with digital local oscillator signals to form band-pass signal at RF. If both the baseband PWM signals and the digital local oscillator signals are binary, this mixing operation is nothing more than a simple logic XOR operation. Another method to simplify this mixing operation is to make the inphase LO take these ternary values of {0, +1, 0, -1}, while the quardrature LO taking the values of {-1, 0, +1, 0}, therefore the digital mixer only outputs these values {-Q, +I, +Q, -I} in sequence. When both I and Q are binary PWM signals, the mixer's output will be binary too. In order to make the LO signals have one of these two formats, the sampling frequency needs to be at 4 times of the LO frequency. The signals from two digital mixers are then combined to form the desired signal at the radio frequency, referred to as RFPWM signal in this paper.

For a signal modulated using PWM, the signal information is carried in the width of the pulse. Since pulse width is defined by the duration time from the rising edge to the falling edge, the transition edges should be preserved after the baseband PWM. However there exists 90 degree phase difference between the inphase LO signal and quadrature LO signal, extra attention needs to be paid to ensure that the baseband PWMs are synchronized with their LO signals respectively. Since the sampling rate is set at 4 times of the LO frequency, the 90 degree phase difference is equivalent to one quarter cycle time difference. The baseband PWM waveforms for inphase and quadrature are

constructed differently: there is an intentional quarter cycle difference being introduced to compensate for the phase difference between the inphase LO signal and the quadrature LO singal. The spectrum plots after each processing steps in the RFPWM are illustrated in [4]. Figure 3 shows the timing waveforms of baseband PWMs and RFPWMs. In this figure, the LO signals take the ternary format, and it can be seen that the combined output RFPWM signal is binary. Additionally, both baseband PWMs are synchronized to the rising edges of their LO signals respectively.

The QAM-PWM modulator presented in this paper uses the quadrature PWM architecture, while INS algorithm is not chosen due to its high computational requirement. A non-recursive noise shaping method is used instead [8].

3. NOISE SHAPING IN DIGITAL PWM

Noise shaping has been widely adopted in over-sampled data converters. The purpose of noise shaping is to generate coarsely quantized signals instead of finely quantized signals, while preserving the SNR performance within a limited bandwidth. In the digital PWM system, noise shaping is necessary since the reference clock would be have inhibitly high frequency had the pulse width been finely quantized, e.g., using 16 bits instead of 8 bits when PRF is 705.6 KHz.

The noise shaping filters used in traditional data converters have been well studied, and most methods can be used in the digital PWM as well. But the noise shaping behavior in digital PWM differs from traditional D-to-A converter, due to the non-linear effects introduced by PWM.

A simulation model was created to compare the noise shaping performance between PWM and traditional DAC as shown in Figure 4. The digital PWM and the traditional DAC use the same noise shaping filter and the same quantizer. The noise transfer functions (NTF) used in this simulation are specified by $H(z)=(1-z^{-1})^N$, where N ranges from 1 to 5. This type of noise shaping filter is not optimal as far as the inband noise suppression performance is considered, but it is sufficient to demonstrate the different behaviors between the PWM and traditional DAC. The effects of analog components in the DAC are not included in the simulation, only the all digital noise shaping loop is considered. The following parameters were selected for the simulation

- Frequency of the input single tone signal = 11 KHz
- Baseband bandwidth = 20 KHz
- Sampling frequency = 705.6 KHz
- Input signal level = -6 dBFS
- Quantization levels = 64

For traditional DAC, the quantization levels indicate the number of bits used in the final DAC, while for PWM, this means the number of high speed clock edges in each pulse cycle. The inband SNR performance from PWM and traditional DAC is summarized in Table 1.

Table 1 Comparison of noise shaping between PWM and DAC

NTF order	PWM SNR (dB)	DAC SNR (dB)
1	63.35	64.03
2	81.03	80.51
3	84.41	92.98
4	73.33	94.51
5	61.34	94.55

It can be seen that the SNR measurements are almost identical between PWM and traditional DAC when the lower order NTFs are used, i.e., N=1 and N=2. When the order of NTF is increased, the SNR trend for PWM differs from traditional DAC:

1. The PWM SNR may not be improved as rapidly as traditional DAC when N is increased from 2 to 3
2. The PWM SNR deteriorates when N is further increased to 4 and 5

The 2nd observation was pointed out in [5] that the quantization noise might be folded back to the baseband if the gain of the NTF is high at the high frequency. We think the 1st observation can be explained by the non-linearity nature of the PWM modulation. However this non-linearity effect can be neglected if only moderate baseband SNR performance is required. Through this simulation model, we formulated our criteria to design a non-recursive NTF filter used for digital PWM system:

1. Minimize the ratio between baseband energy and total energy when the filter's input is white noise.
2. The filter coefficients should satisfy minimum phase, 1-norm requirement, and its 1st coefficient should be unity. These conclusions are provided in [8] with details.
3. The filter gain at high frequency ($\omega=\pi$) should be limited. This requirement is derived from the above simulation results.

These criteria can then be formulated mathematically as follows. Assume an N-tap FIR filter with coefficients **h**, where $\mathbf{h} = \{h_0, h_1, \ldots, h_{N-1}\}^T$, the baseband energy can be calculated by

$$E_b = \int_0^{\omega_b} \left| H(e^{j\omega}) \right|^2 d\omega = h^T R h \tag{1}$$

wherein **R** is a matrix, and

$$r_{m.n} = \begin{cases} \omega_b, m = n \\ \dfrac{\sin(n-m)\omega_b}{n-m}, m \neq n \end{cases} \tag{2}$$

The total energy can be calculated using Parseval's theorem, i.e.,

$$E_t = \sum_i |h_i|^2 \tag{3}$$

Therefore the optimized NTF should try to minimize

$$J = \frac{(E_b)^{\alpha}}{(E_t)^{\beta}} \quad (4)$$

The parameter α and β are used as weighting factors when performing the optimization. The object function should be minimized subject to these conditions:

- The 1-norm of **h** should be bounded, which is dependent on the number of levels in the quantizer, i.e.,

$$\sum_{i=0}^{N-1} |h_i| \le q \quad (5)$$

- The filter should be minimum phase, i.e., all the zeros of the filter should be within the unit circle
- The gain at high frequency should be bounded, i.e.

$$\sum_{i=0}^{N-1} (-1)^i h_i \le b \quad (6)$$

The all digital transmitter to be demonstrated is specified to have 10 MHz baseband bandwidth, and the PRF is chosen to be 100 MHz. The center frequency is 800 MHz; therefore the frequency of the high speed reference clock is 3.2 GHz. The prototype implementation uses an 8 tap finite impulse response (FIR) NTF designed using this method.

4. HARDWARE PROTOTYPING AND MEASUREMENTS

As described in section 2.1, the entire signal processing algorithms required by digital PWM is running at the frequency of PRF. The only high speed circuit required is the final PWM waveform generation. Therefore it is feasible to prototype an all digital QAM-PWM modulator on an off the shelf FPGA device.

The architecture of the digital QAM-PWM modulator is shown in Figure 5. Only the block diagram of the inphase path is shown in detail; however the quadrature path should consist of almost identical architectural blocks. The QAM modulator consists of one QAM symbols generator whose symbol rate is 5.057 MHz, one interpolation filter to upsample the sampling rate to 16 times of the symbol rate, and one sample rate converter that converts the sampling rate to the 100 MHz PRF. The details of this QAM modulator are provided in [9]. The digital PWM consists of one natural sampler, one quantization with noise shaping block, and one PWM waveform generator. The natural sampling algorithm [6] consists of only feed-forward data-paths; therefore it can be pipelined fairly easily. The quantization with noise shaping block has feed-back paths, therefore is more difficult to implement even though the PRF is merely 100 MHz. The FIR NTF filter is realized using the transposed struccture, combined with retiming technique and canonic signed digit (CSD) conversion of some coefficients. The mixing between LO signals and all the possible baseband PWM signals were pre-computed and stored in a ROM. This ROM is addressed by the quantization output, i.e., the quantized pulse width. The selected RF PWM waveforms from inphase path and quadrature path will be combined before the high speed serializer generates the 1 bit RF signal.

The FPGA device chosen for the prototype is Xilinx's Virtex2pro: XC2VPX20-FF896, speed grade -7. This FPGA has on chip multi-gigabit transceiver (MGT) which is used as the high speed parallel to serial converter to generate binary signal at 3.2 GHz. In Table 2, the logic resource allocation is broken down for the QAM-PWM modulator implemented on this device.

Table 2 Logic resource allocation for QAM-PWM modulator

Logic Elements	PWM	QAM
REGISTER	787(26.1%)	2221(73.5%)
LUT	2447(47.7%)	1833(35.7%)
MUXCY	2052(67.1%)	1008(32.9%)
XORCY	1958(66.8)	973(33.2%)

The logic elements allocation results are extracted from Synplcity synthesis results. The final place and route tool reports that the entire QAM-PWM design utilizes 18 multipliers (20%), 4 RAM16s (4%), and 3911 slices (39%). The percentage number in the parenthesis is the percentage with respect to the total available resources on this FPGA.

The spectrum and EVM measurements are shown in Figure 6. While the pass-band noise floor is about 45 dB down from the signal, more aggressive noise shaping technique can be used to achieve better pass-band noise performance. However the computation requirement for that case might prevent it being implemented, at least using the off the shelf FPGA device will be very difficult. The EVM measurement is less than 1%, which is almost identical to the EVM measured at the output of QAM [9].

5. SUMMARY

An all digital QAM-PWM modulator is presented in this paper. To the best of the authors' knowledge, this work is the first demonstration of real time digital RF PWM signal synthesis, especially using an off the shelf FPGA device. The fundamental operations for digital PWM are briefly discussed, including natural sampling and quantization with noise shaping. The noise shaping of digital PWM differs from traditional DAC converter based on simulation results; therefore the NTF for digital PWM needs to be designed using additional restrictions. A design method is formulated based on the observation from simulation, and one design example is presented based on our QAM-PWM modulator

requirements. This type of NTF is chosen mainly because of its less computation requirement. The QAM-PWM modulator's architecture and performance measurements are presented at the end.

6. ACKNLEDGEMENT

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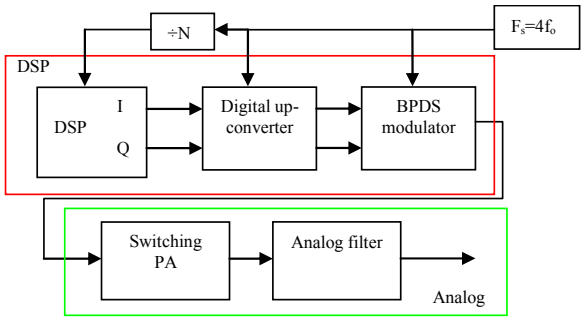

Figure 1 Digital transmitter using BPDS

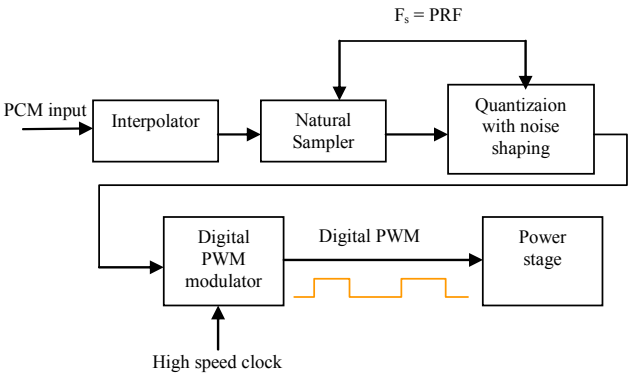

Figure 2 All digital transmitter using PWM

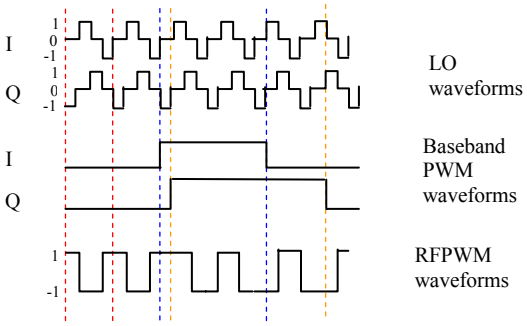

Figure 3 Digital RFPWM timing diagram

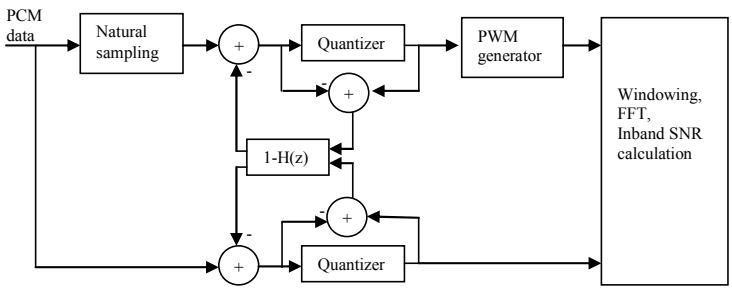

Figure 4 Simulation to compare noise shaping behaviors of PWM and traditional DAC

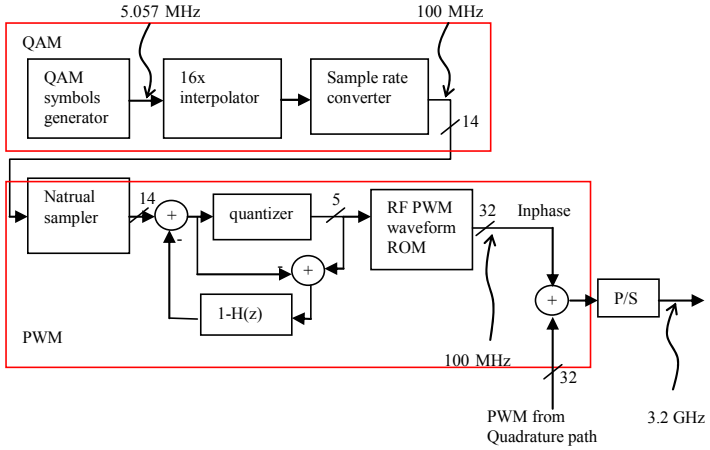

Figure 5 Architectural diagrams for all digital RFPWM prototype

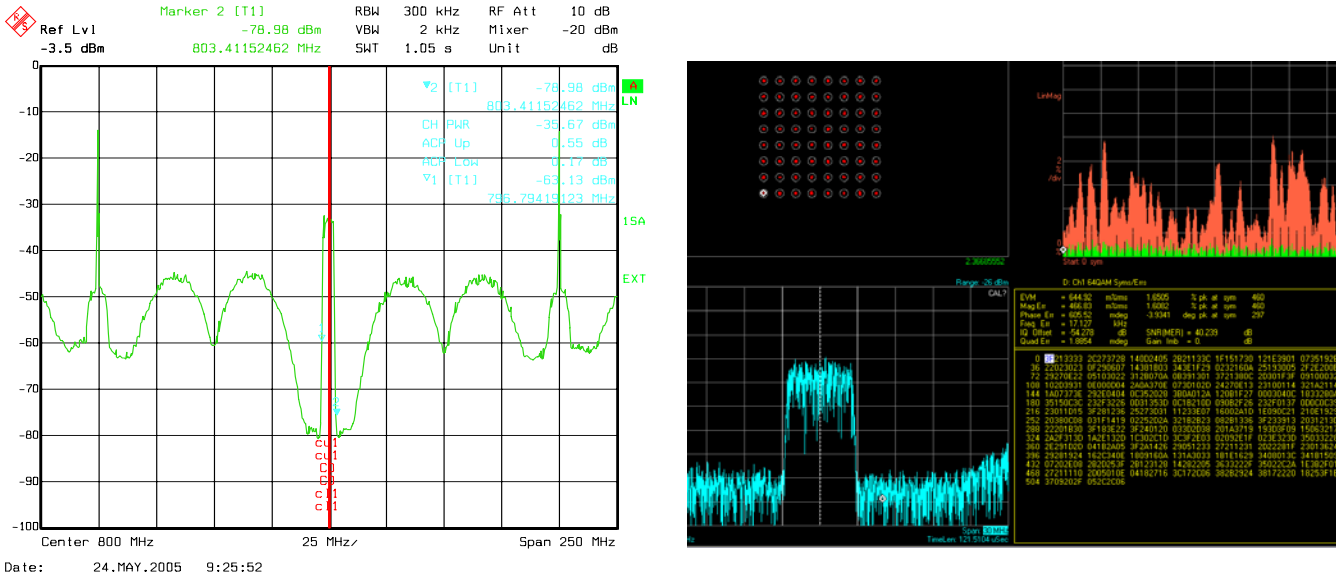

Figure 6 Measurements of RFPWM: wideband spectrum and EVM