SIGNAL PROCESSING IN WIRELESS COMMUNICATIONS – THE CASE FOR THE HIGHEST CLOCK SPEEDS

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ABSTRACT

HYPRES superconducting integrated circuits are able to sample input signals and process the data at clock speeds as high as 40GHz at the current (1500nm) fabrication node. This enables new hardware and software architectures in wireless communication systems. The following possibilities are considered in this paper.

- ADC & DAC operations at 40GHz offer the potential of highly frequency agile basestations able to support multiple handsets in multiple bands simultaneously.
- On-chip correlation circuits clocked at the same 40GHz frequency enable monitoring of multi-GHz bandwidth signals for signal intelligence applications
- Closely integrated on-chip RF DSP and ADC & DAC operations allow ultra fast demodulation, correlation and re-modulation for co-operative networks of terminals which benefit from the ultra short pipeline delay between reception and retransmission
- Multiuser detection algorithms in CDMA

1. INTRODUCTION

CMOS scaling continues to deliver higher and higher transistor counts on each chip as the 65 and 45nm process nodes move towards commercial introduction. However, the increase in clock speed that used to come with each new process generation has slowed dramatically since the 130nm node and shows no sign of renewing it's vigor. To deal with this, chip architects and algorithm developers are looking to parallelization and multi-core technologies to maintain the pace of performance improvement. For many applications this is an acceptable solution; however some problems are inherently serial in nature, must be carried out very rapidly, or require iterative algorithms to solve them. Using chips with significantly higher clock speeds is the only way to enable these applications.

This paper identifies some problems of this type and describes developments at HYPRES and Chalmers University to solve them.

2. FAST, WIDEBAND ADC DEVICES

Analog-to-Digital (ADC) devices for most communications systems are required to deal with interfering signals significantly larger than the wanted signal. This places demands on the ADC that have traditionally only been met by slowing down the sample rate of the device and restricting the maximum bandwidth that can be digitized. For software radio systems that offer flexibility as a key benefit this is a major problem since it prevents operation in multiple bands via the same radio. The only solution is to have parallel radios, each tuned to a specific band, and some form of MAC (Media Access Control) and system controller to coordinate the multiple radios. A much more elegant solution is a single radio linked to a tunable filter or bank of filters where required.

Current Hypres ADC devices sample at 20GHz to 40GHz. It can be seen in Figure 1 that very high linearity has been demonstrated for superconducting converters, including a SINAD of >121dBc at 400KHz for a device delivered to the US navy [1] and is the highest dynamic range ever reported for an ADC at this frequency (to the authors knowledge). Other superconductor-based ADC devices offer impressive specifications at higher frequencies using a highly oversampled $\Sigma\Delta$ architecture made possible by the very high clock rates of superconducting devices. The blue solid line in Figure 1 shows the performance from the 400KHz optimized device (a Δ converter) and the green line is a 13GHz $\Sigma\Delta$ device. The dotted lines are the performance Hypres expects from superconductor ADC devices over the next 2-3 years. Higher order feedback loops are expected to improve noise shaping and higher order quantization at the 40GHz sample rate offers another jump in performance. Higher order quantization may limit the maximum SFDR as the price for much higher resolution in the 400MHz

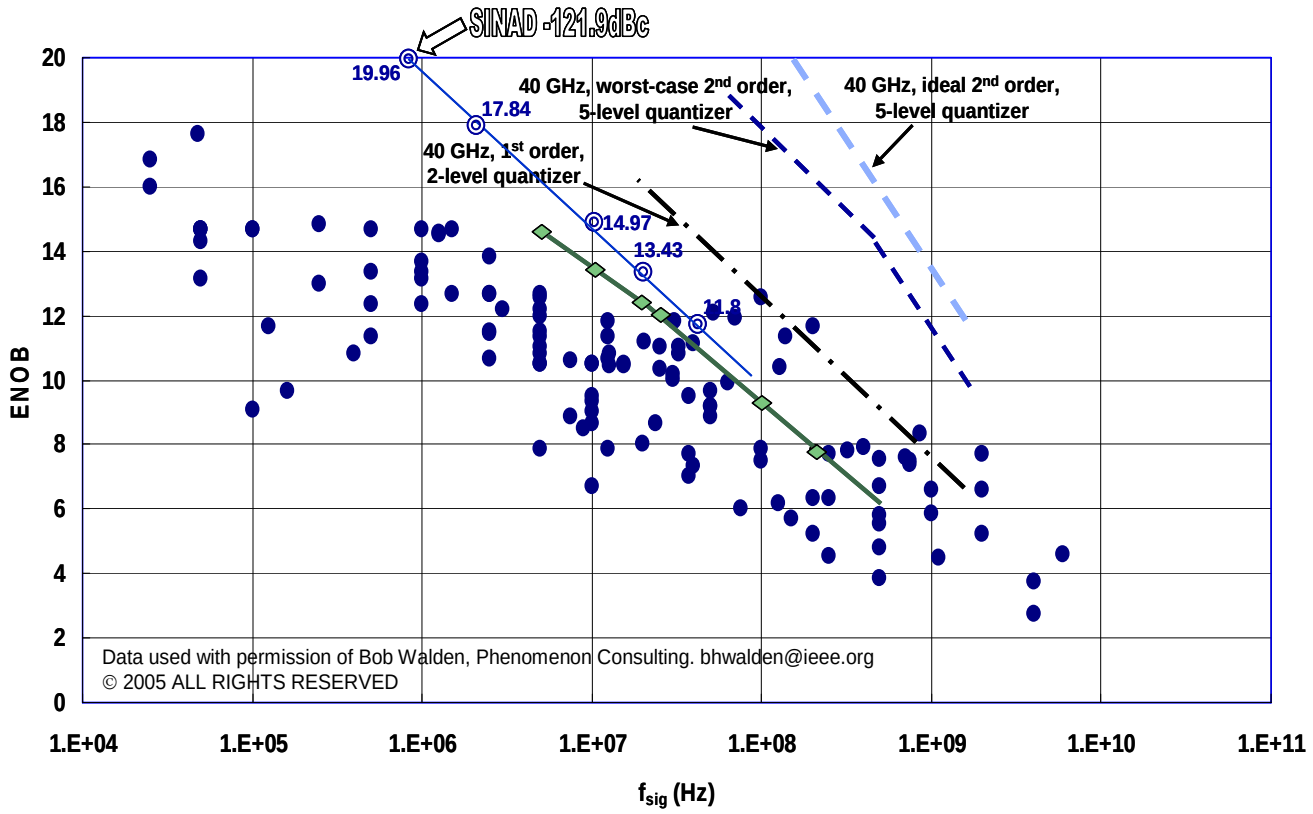

Figure 1 HYPRES ADC performance compared to a selection of semiconductor ADCs. Solid lines represent devices already made by Hypres and the dotted lines are expected performance improvements.

bandwidth but we expect to be able to optimize our designs for all the major markets to provide the best performance trade-off for each application. For a more complete account of this technology see [2].

3. ULTRA WIDEBAND CORRELATING RECEIVERS AND CONCEALED WIDEBAND COMMUNICATION

Signal intelligence agencies seek to monitor the widest spread of frequencies possible. This is currently achieved using banks of filters and downconverters (radios) which must be downconverted and monitored in parallel. This multiple "radio" architecture works well for signals with a narrower bandwidth than the individual receivers but fails when the signal energy is spread over bandwidths covered by multiple receivers. The use of superconducting wideband receivers together with correlators running at a similar speed gives the SIGINT systems operator greater confidence that any signal transmitted by an adversary can be detected.

The problem can be turned around and used to give an advantage to an organization using high speed superconducting technology for secure communications. A spectrum spreading device running it's multipliers at a 40GHz clock speed can spread a signal over 20GHz of spectrum to render it completely undetectable to an eavesdropping device. New techniques will be necessary to amplify and broadcast a signal of this bandwidth and the frequency selective nature of the channel that the signal is transmitted over will need to be well understood. However, superconducting digital hardware offers the only viable platform to support this type of communication.

4. RAPID MODULATION AND DEMODULATION FOR COGNITIVE RADIO NETWORKS

There has been a lot of innovative work in the field of cooperative radio networks in recent years [3] but many of these algorithms and techniques rely on the ability of a transceiver to rapidly demodulate, process, re-modulate & transmit a signal with the network level benefits falling as this time rises. By tightly coupling the ADC / DAC & digital processing in a single all digital system clocking at 40GHz the Hypres direct conversion architecture cuts this

time by a factor of 40 or more when compared to current DSP & FPGA solutions.

5. MULTI USER DETECTION FOR CDMA

Multi user (or joint) detection receivers are known to provide large capacity benefits in CDMA based systems. There is a large and growing literature in this field which is beyond the scope of this paper but a good review article can be found in [4]. They work by treating the noise power in the channel bandwidth (caused by users other than the user of interest to a particular receiver) not as noise but as signals that can be processed along with the signal of interest. This has the effect of lowering the noise floor and allowing many more users to share the same spectral bandwidth. Field trials and system simulations have shown that uplink capacity in UMTS systems can be increased 35% in realistic multi-cell systems compared to conventional RAKE receivers [5]. This data is given for the Parallel Interference Canceller that has low coverage rate and problems with stability. The Successive Interference Canceller potentially can give even greater increase in performance. Successive iterative algorithm with soft decision between iterations is stable, power control independent and has fast convergence rate. Supporting this form of signal processing in real time for a commercially interesting number of users is beyond the capability of current signal processing hardware. As a result, Chalmers University & Hypres are engaged in a program to develop a Digital Signal Processor to demonstrate support for this function and enable further trials and eventual commercial deployment. Simulations have been done to determine the processing speed required to support a parallel interference cancellation algorithm as the number of users varies [6]. The results of this simulation are shown in Figure 2 for different user data rates. It can be seen from this that there is a close correlation between maximum processing speed that can be supported in hardware and the number of users that can simultaneously transmit in a cell. The data is for WCDMA in a realistic multipath propagation environment. The reduction in the noise floor can also be used to increase the range of a cell in coverage limited applications. For wireless operators in developed countries as little as 15% of the cost of running a network is related to the cost of the electronics. Most of the rest is site rental, maintenance access, civil engineering, power etc. so there is substantial value in any system that can reduce the number of basestations required to cover a given area either by range extension or capacity expansion.

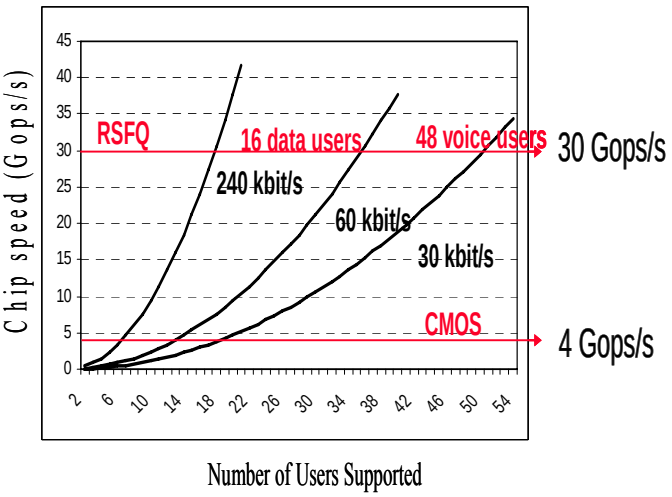

Figure 2. Simulation of the number of users that can be supported in a UMTS cell depending on the speed of the hardware supporting the multi-user detection algorithm. It can be seen that increasing the speed of the processor from 4 $GOPs^{-1}$ to 30 $GOPS^{-1}$ increases the number of supported voice users by a factor of 2.4

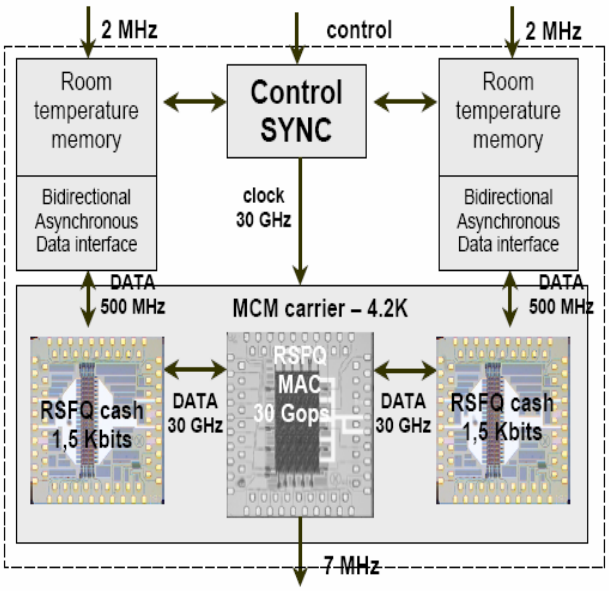

Figure 3. Actual block diagram of the superconducting digital signal processor supporting 30 GOPS speed

6. REFERENCES

[1] Work funded in part by the Office of Naval Research & the US Department of Defence.

[2] O. A. Mukhanov, D. Gupta, A. M. Kadin, and V. K. Semenov, "Superconductor Analog-to-Digital Converters", Proceedings of the IEEE, vol. 92, no. 10, pp. 1564-1584, October 2004

[3] http://people.deas.harvard.edu/~vahid/Pre-prints.html

[4] S Moshavi "Multi-User Detection for DS-CDMA Communications" IEEE Communications Magazine, October 1996, p124 – 136

[5] Gunnarsson & Hagerman IEEE Signal Communications. To be published

[6] H. Zhao, T. Ottosson, E. Ström, A. Kidiyarova-Shevchenko, K. Platov, "A Fixed-Point Implementation of Successive Interference Canceller for WCDMA", presented at CIC 2003.