SUPERCONDUCTOR DIGITAL-RF TRANSCEIVER COMPONENTS

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ABSTRACT

Superconductive technology offers unparalleled digital and mixed-signal circuit performance, advancing digital processing from baseband to RF stages. This allows elimination of analog filters and mixers with generally poorly controlled phase performance, causing intersymbol interference limiting an overall communication system performance. HYPRES has been developing superconducting circuit components for application to digital RF communication transceivers. The components include low-pass and band-pass analog-to-digital converters, digital decimation and correlation-based filters, digital up/down-converters, and low-time-jitter clock sources. All of these are based on ultra-fast Rapid Single Flux Quantum (RSFQ) digital circuits, with clock rates up to 20 GHz demonstrated with 3-micron technology, and being scaled to 40 GHz and above. In this paper, we will discuss design and performance of some of these components.

1. INTRODUCTION

The critical feature of software-defined radios (SDR) is the ability to process wide range of frequency bands, channel bandwidths, and different protocols. Instead of multiple radios with dedicated narrow-band transceiver channels, a single software-reconfigurable radio employing a wide-band, multi-standard transceiver will be used. Such radio will also enable synergy among different applications (communications, EW, SIGINT, radars, etc.).

However, practical realization of this true SDR presents a host of technical challenges. The wide bandwidth requirement means that such a transceiver will be left open to a large number of carriers, potentially creating an overlapping picture of co-channel interferences, aliases, and intermodulations. The requirement of simultaneous handling under software control of a large number of signals with different coding, protocols, hopping-patterns, etc. implies that the inflexible analog front-end components would be replaced by very high speed digital parts bringing the digital domain as close to the antenna as possible.

To meet these requirements, a true-SDR-compatible transceiver must require mixed-signal and digital components capable of delivering extreme speed, linearity, dynamic range, noise, and sensitivity performances. Neither conventional analog-to-digital and digital-to-analog converters (ADCs and DACs) nor conventional digital signal processing (DSP) circuits have the necessary performance. On the other hand, it has recently been shown that the unique features of superconducting electronic technology lead to ultrafast circuits with the performances that can make true digital-RF processing possible [1].

2. SUPERCONDUCTIVE TECHNOLOGY

Modern superconductor electronics is based on Rapid Single Flux Quantum (RSFQ) technology [2-4] which relies on a fundamental quantum mechanical property of superconductors. In a closed section of superconductor material magnetic flux can exist only in discrete, quantized amounts. These amounts are multiples of the *magnetic flux quantum* (Φ_0), a fundamental physical constant equal to

$$\Phi_0 = h/2e \approx 2.07 \times 10^{-15} \text{ Wb,}$$

where h is Planck's constant and e is the electron charge. When a single flux quantum (SFQ) moves through a superconductor circuit consisting of Josephson junctions and inductors, it is appears as a voltage pulse – an "SFQ pulse" – with a constant integrated area given by

$$\int V(t)dt = \Phi_0 \approx 2.07 \text{ mV·ps.}$$

The RSFQ technology defines a convention for using these SFQ pulses to perform logic and arithmetic operations. For carrying out digital processing, Adders, multipliers, clocks, registers, and data buffers, all the components necessary for carrying out digital processing have been developed, with active delays to control time synchronization precisely. The diversity of components that have been developed has brought RSFQ technology to the point where the design of larger systems such as a transceiver can be reasonably considered, to take advantage of fundamental superconductive technology features:

A) Quantum Accuracy – RSFQ technology, based on quantum phenomenon, can convert signals between analog and digital domains with extreme linearity. This

fundamental accuracy demonstrated by the world's primary standard for voltage is used to implement accurate thresholds in superconductive DACs.

B) Ultra-High Speed – even with a 3-μm fabrication process, complex circuits have been demonstrated, including basic logic gates at 100 GHz and large-scale ICs at 20 GHz. Sub-micron (0.3-μm) logic gates (toggle flip-flops) in the RSFQ technology have even been experimentally demonstrated to operate at >750 GHz [5].

C) Dispersion-Less Transmission Lines – superconductor microstrip lines allow fast ballistic transport of picosecond pulses of data and clock between logic blocks, circumventing the problem of interconnect delays that dominate the overall speed of semiconductor ICs.

D) Low Noise – cryogenic (4 Kelvin) operation ensures reduced thermal noise (75 times smaller than room temperature). Lower receiver noise temperatures allow detection of smaller signals.

E) Low Power – switching energy of Josephson junctions is of the order of 10^{-18} Joules. Even at 100 GHz speeds, the on-chip dynamic power consumption is in the μW range. Static power consumption, proportional to the number of devices, is <1 mW for circuits with thousands devices. This low power dissipation allows very dense packaging of chips.

F) Radiation Hardness – the all-thin-film fabrication technology used for superconducting electronics is intrinsically radiation hard, impervious to soft errors due to single particle events.

Simple Low-Cost Fabrication – because RSFQ ICs are built by an *all-thin-film* process, both the development and fabrication cost per wafer is considerably lower than other semiconductor technologies.

Commercial cryocoolers have recently become available that can reliably maintain the needed cryogenic temperatures with only electric power needed. Similar cryocoolers, fielded in commercial wireless base stations for cooling superconducting passive filters, have proven to be extremely reliable (with a projected MTBF of 90 years [6]). Further improvements in size, price, and power of these cryocoolers are expected.

3. DIGITAL-RF TRANSCEIVER ARCHITECTURE

Our design is based on the "digital-RF" approach, meaning performing signal conversion and digital processing at RF rather than conventional baseband. In this approach, the analog filter and up/down-conversion stages from/to lower IF or baseband are eliminated. The digital-RF architecture is illustrated in Fig. 1 using an example of a receiver. Input wide-bandwidth RF signal is applied directly to an ADC modulator producing an oversampled low-bit-width digital code at very high data

rate (e.g. 20 or 40 Gbps). This high-rate data stream is processed before down-conversion using a relatively low-complexity but very high-throughput processor (RF DSP) to implement various functions such as digital signal combining from multiple channels, true-time delay for digital beamforming, adaptive active cancellation of transmit channels, correlation-based digital filtering, etc., if necessary. Finally, this high-rate data is down-converted to baseband using digital mixers and decimation filters for further processing and decoding. Clearly, such an architecture can be realized only if both ADC and DSP can deliver sufficient performance and can operate at very high clock rate (e.g. 20 or 40 GHz).
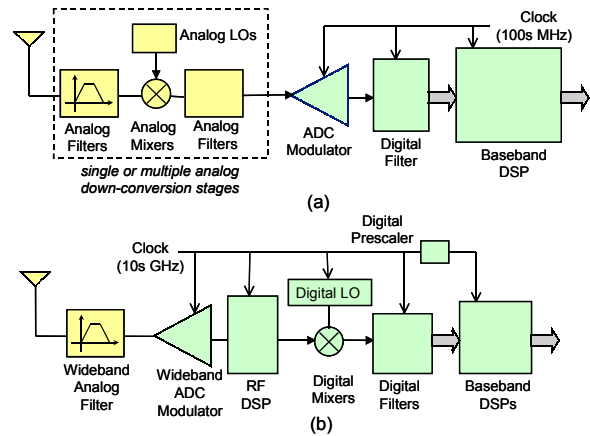

Fig. 1. Comparison of (a) conventional and (b) digital-RF receiver architectures. In the digital-RF scheme, signal conversion is carried out directly at RF frequencies using a wideband ADC modulator with large oversampling. The digitized RF low-bit-wide data are then processed at very high data rates at RF DSP before being digitally down-converted and filtered to baseband for further processing.

The Digital-RF design principle can be extended to a whole transceiver. Fig. 2 shows an example of such a transceiver clocked with an integrated low-jitter high-speed (e.g. 20 or 40 GHz) SFQ clock and synchronized with external low-speed (20 MHz) reference clock using PLL. In the receiver chain, the RF signal from the antenna is filtered, (possibly) amplified, and then sent directly to an ADC. The down-conversion is carried out digitally, in a way that can be easily reprogrammed. A digital decimation filter is used to decrease the output bandwidth, while increasing the effective number of bits. This can be a quadrature receiver or be channelization into multiple baseband channels, as described in [7].

The transmitter part carries out the same digital functions in reverse. A fast DAC is clocked by a high-speed SFQ clock and generates spectrally-pure RF signals to be amplified by a high-power amplifier (HPA). The diagram also shows a dynamic digital equalizer, a digital predistortion module that is combined with the DAC to

compensate for nonlinearities in the HPA. Since multiple channels can be combined digitally into one broadband digital-RF signal before amplification, only a single multi-carrier HPA is needed.

All fast digital and data conversion processes shown in Fig. 2 will be carried out using RSFQ low-temperature superconductor (LTS) circuits cooled to cryogenic temperatures ~ 4 K, as indicated by shading in the figure. The analog filtering and duplexing can be carried out at an intermediate cryogenic temperature (~ 60 K) in order to minimize thermal noise. The HPA and back-end processing will be implemented using conventional semiconductor parts and placed at ambient temperature. This hybrid configuration is compatible with available commercial cryocoolers, which employ two or more different temperature stages.
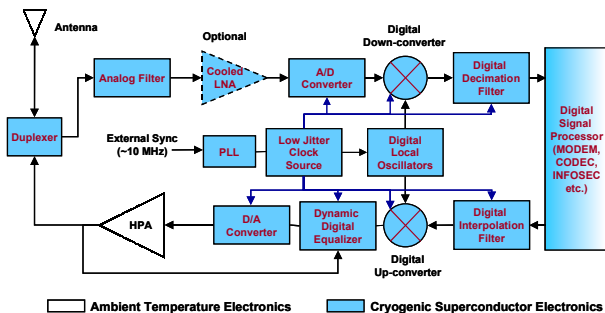

Fig. 2. Block diagram of digital-RF transceiver, where data conversion is carried out directly at RF frequencies, and signal processing is done using ultra-fast superconducting digital RSFQ circuits operating at tens of GHz (e.g. 20 or 40 GHz).

4. RECEIVER COMPONENTS

4.1. Analog-to-Digital Converter

An oversampling ADC modulator is used in our digital receiver. This modulator produces quite large quantization noise but samples the signal many times, i.e. works with a large oversampling ratio. We make the quantization noise small by digital filtering, which can take advantage of these very large oversampling ratios available to us due to the extremely high-speed ADC modulators and digital logic possible in superconductivity.

We have been developing low-pass and band-pass ADC designs using delta and delta-sigma modulator approaches. Fig. 3 shows a 15-bit low-pass ADC chip comprising a delta modulator and decimation digital filter operating at 19.6 GHz clock [8]. This ADC design is based on a phase-modulation-demodulation technique uniquely developed using RSFQ technology. In this technique, a derivative of the analog signal modulates individual delays of SFQ clock pulses within each clock period. The phase demodulation is performed by a race arbiter producing 2- or 4-bit thermometer code depending

of the number of arbitration bins. Then, the digitized data stream is passed to a digital decimation filter with programmable decimation ratio. Fig. 4 shows the measured data of this ADC chip taken at ~13 GHz clock. This low-pass delta ADC design can be naturally transformed to a band-pass sigma-delta design. Fig. 4 shows the projected performance of RSFQ band-pass sigma-delta ADCs being currently implemented.
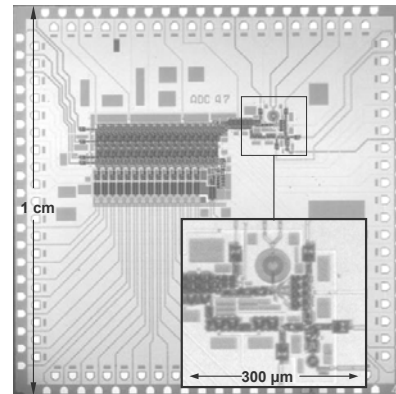

Fig. 3. A 15-bit ADC chip consisting of low-pass delta modulator (in the insert) and decimation digital filter operating at 19.6 GHz clock. The 10×10 mm^2 chip contains about 6,000 Josephson junctions.
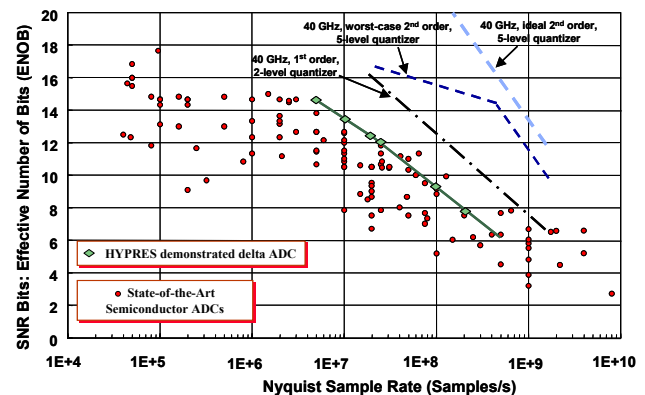

Fig. 4. Measured SNR performance of low-pass delta ADC contrasted with state-of-the-art semiconductor ADC and projected performances of RSFQ sigma-delta designs.

The ADC front-end is the ultra-sensitive superconducting quantum interference device (SQUID), which is commonly used in the most sensitive measurements of magnetic field and current. In many applications, the ADC front-end is sensitive enough to eliminate the need for the low-noise amplifier (LNA). Since superconducting electronics operates at cryogenic temperatures (4-5 K), the thermal noise contribution is also reduced significantly compared to room-temperature receivers. Furthermore, a superconductor thin-film transformer used as a signal input device can work as a

very effective power limiter protecting ADC circuitry from input power surges.

The RSFQ chips enable simultaneous wideband and high-fidelity digitization because the digitization levels are set by a ratio of fundamental physical constants ($h/2e$) rather than component matching, as in traditional designs. This unique feature gives the ADCs the capability of producing 14 to 20 effective (true) bits with better than 100 dB spurious-free dynamic range (SFDR) over the entire communications spectrum from 100 kHz to 2 GHz.

4.2. Digital Filters

4.2.1. Decimation Filter

When the precise waveform of the signal of interest is not known, but the frequency band of the signal of interest is known, decimation digital filtering is used to extract this frequency band. This is done by a linear process of multiplication of the incoming signal by a window filter function, and building up signal-to-noise ratio (SNR) by removing noise power located out of the band of interest. The chip shown in Fig. 3 contains a 15-bit decimation filter built using a cascaded integrator comb (CIC) architecture. This 20 GHz first-order filter has two integration stages and one differentiation stage. The first integration stage is necessary to restore the signal from differential code while the other stages do low-pass filtering. The filter is equipped with a programmable decimator module allowing dynamic trade-off between bandwidth and SNR. The filter design is made in a highly modular fashion allowing easy reconfiguration and expanding to higher orders.

4.2.2 Correlation-Based Matched Filter

When the waveform of the signal of interest is known, it becomes possible to use a matched filter based on correlation to perform digital filtering in the frequency and time domains simultaneously. Such a correlation filter will process out all noise that is not correlated. Signal power remains unchanged while noise power decreases in the correlation process. Other signals that the correlator is not programmed to correlate are similarly decreased in a noise-like manner.

In spread-spectrum communication systems, correlators are widely used. The main difference between them and our correlator receiver is that we propose to correlate the RF waveform itself, while the usual schemes perform correlation on the demodulated digital waveform (chips) in baseband. Therefore, in our case the correlator must work at the high-speed sampling clock rate (e.g. 20-40 GHz). High-speed RSFQ technology makes it possible to operate correlators at such rates.

For correlation to work properly, the waveform reference template must be synchronous with the received waveform. To achieve this phase synchronization, we use a pair of correlators phase shifted by $\pi/2$ (Fig. 5). If the two waveforms – the received waveform and the reference template – are in phase, one of the correlators (in-phase) will produce a maximum signal while the other (quadrature) produces a minimum. The phase synchronization technique is a feedback scheme that maintains the quadrature correlator output at the minimum by advancing or retarding the phase of the waveform template. In the digital domain, the phase adjustments are achieved in discrete time steps, corresponding to single clock periods. The number of required correlator channels depends on the symbol constellation of digital modulation scheme (e.g. 4 for QPSK, 16 for 16-PSK, etc.).
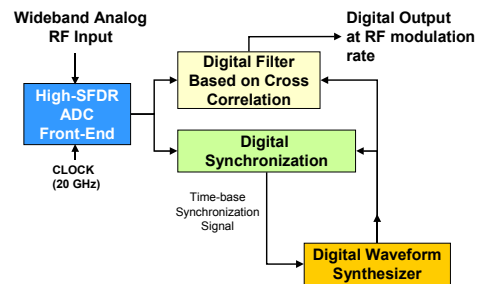

Fig. 5. The ADC front-end (modulator) produces a high-fidelity digitized RF waveform, which is correlated against the corresponding digital reference template waveform.
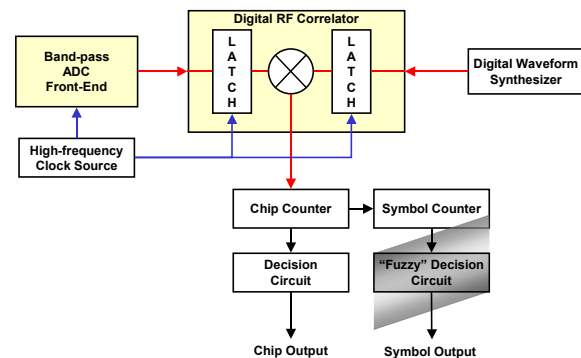

Fig. 6. The simplest 1-bit implementation of a correlator. The counter can be split into two parts, corresponding to chip interval and symbol interval respectively, producing both chip and symbol outputs, corresponding to demodulation and de-spreading. The binary decision circuit may include the probability associated with each decision.

If we use a single-bit delta- or delta-sigma ADC modulator, the correlator-based matched filter can be implemented using just a single-bit hardware. Fig. 6 shows a 1-bit cross-correlator that correlates the digitized data stream to the waveform template. Only one correlation stage required if the two digital waveforms are perfectly synchronized. Multiple (3 to 5) correlation stages can improve tolerance to imperfect synchronization. The correlator output, integrated over the

chip duration yields a correlation sum corresponding to the chip value, determined by a binary decision circuit. The chip counter output can be further integrated over the duration of a symbol to yield the symbol value through a similar decision circuit.

The "fuzzy" decision circuit produces outputs "0" and "1" with associated probabilities. Normally, the counter output will be a number between 0 and N, where the count of 0 or N correspond to two binary symbols. However, because of errors induced by channel noise, phase synchronization error etc., the counter output will often lie between 0 and N, requiring a multi-bit decision circuit.

4. CLOCK SOURCE

On-chip, high-frequency clock sources are essential for the achieving higher performance of the transceiver. We have developed ultra-low time jitter clock sources for RSFQ digital circuits using high-quality long Josephson junction (LJJ) resonant oscillators. To meet the requirement for time-interleaved SFQ clock signals of complementary phase, two-phase 30 and 50 GHz clock sources using LJJs have been developed with both linear and annular geometry [9]. The generated SFQ pulses can be easily distributed to RSFQ circuits with negligible distortions using superconductive transmission lines. Unperturbed by reflections from boundaries and collisions among the fluxons (flux quanta), the annular LJJ oscillator has demonstrated superior stability and higher quality factor ($>10^6$) than the linear LJJ oscillator [10].
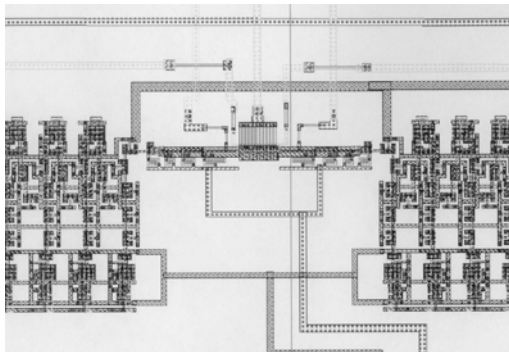

Fig. 7. The layout of linear LJJ oscillator coupled to two chains of RSFQ binary frequency dividers.

The LJJ oscillator with linear geometry is easier to interface with RSFQ circuitry since it has well-defined boundaries at either end, facilitating a two-phase SFQ clock source (Fig. 7). On the other hand, multiple clock phases may be derived from an annular LJJ oscillator by connecting interface circuitry at various points around the circular junction, if the interface circuitry does not interfere with the fluxon(s) in the annular junction. This

clock generator has been demonstrated a 60 fs (0.06ps) time jitter during independent tests at the University of Rochester [11].

TABLE I
COMPARISON OF DIFFERENT JOSEPHSON JUNCTION OSCILLATORS

OSCILLATOR TYPE	QUALITY FACTOR ($f/\Delta f$)	TYPICAL FREQUENCY
Single small junction	100 - 1000	> 100 GHz
Array of small junctions	10^3-10^4	> 100 GHz
Long junction in flux flow mode	~10^3	> 100 GHz
Ring oscillator	1000 - 5000	10 – 20 GHz
Long junction in resonant mode	$10^5 – 10^6$	10 – 100 GHz

5. TRANSMITTER COMPONENTS

5.1. Digital-to-Analog Converter

On the transmit side, the waveform is processed completely in the digital domain up to RF before converting to an analog form with an ultra-linear RF DAC. We have developed an RSFQ dual binary-type DAC utilizing a unique combination of binary digital-to-frequency converters (DFC) and binary summing SFQ arrays (Fig. 8). Although this DAC chip was designed for low-frequency metrological application, it can be naturally extended to higher speed. By exploiting the ac Josephson effect, each SFQ pulse train from the DFCs will generate an output voltage across the corresponding serial stage of the SFQ summing array. The sum of the induced voltages from all stages appears at the analog output.
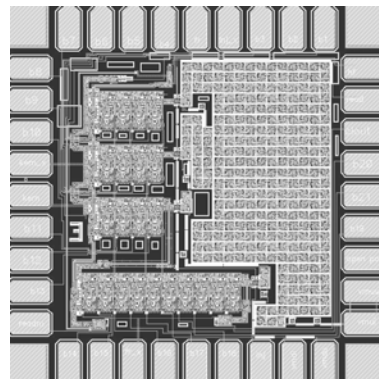

Fig. 8. An 18-bit RSFQ DAC chip. The 5x5 mm^2 chip contains more than 2,000 Josephson junctions.

5.2. Amplifier Linearizer

Perhaps the most powerful impact of the digital-RF approach will be in the area of linearization of high-power amplifiers (HPAs), which inevitably exhibit significant intermodulation distortion, especially near their maximum output powers. Unlike conventional baseband or intermediate frequency (IF) predistorters, which are limited to narrowband correction of slowly varying non-linearities, our RF predistorter can correct instantaneous, signal-dependent fluctuations of the HPA transfer function on a sub-nanosecond time scale. Only RSFQ technology is fast enough to perform direct digital predistortion of RF.

Fig. 9 shows a block diagram of our digital-RF predistorter scheme. After digital up-conversion, the multi-bit digital RF waveform is encoded into a single oversampled bit-stream, e.g. delta-sigma code. This code is fed into a sigma-delta DAC, the output of which is amplified by a chain of successively higher power amplifiers. The predistortion involves adding or subtracting pulses in the sigma-delta code stream. In RSFQ technology, this means adding and subtracting SFQs into an integrating loop, coupled to the DAC. The quantum nature of RSFQ DAC ensures perfect linearity.
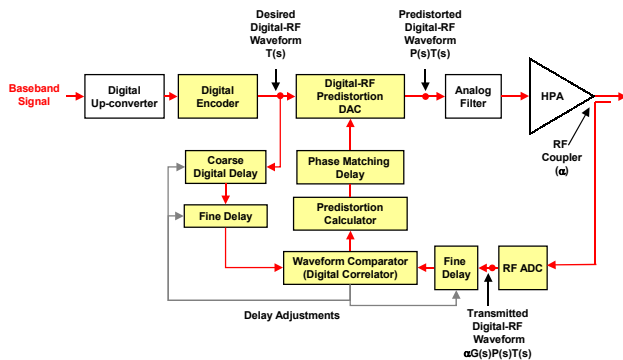

Fig. 9. Digital-RF predistortion scheme.

In the feedback path, the ADC modulator (e.g. a bandpass sigma-delta circuit) produces a stream of SFQ pulses at the sampling clock rate. This allows sample-by-sample comparison of the original digital RF transmit waveform and the distorted digital RF waveform, obtained by digitizing a fraction (α) of the amplifier output through an RF coupler. The waveform comparator is essentially a digital cross-correlator. It can be implemented as a single exclusive-OR (XOR) gate, followed by an accumulator to keep a running sum over some time period. The sample-by-sample comparison requires precise matching of the original and the distorted waveforms. RSFQ coarse and fine delay elements allow delay matching with a fractional clock period accuracy by adjusting the bias of active Josephson transmission lines (JTLs). The predistortion calculator calculates the amount addition or subtraction of SFQ pulses based on the

running sum obtained by the waveform comparator. A fixed phase matching delay is needed to ensure proper phase matching of the feedback signal with the RF signal. This delay may be calculated during a calibration cycle, where an un-modulated RF carrier is transmitted.

6. CONCLUSIONS

The Digital-RF design approach has radically transformed the architecture of a transceiver by bringing the power of digital processing to RF. Practical implementation of this approach is enabled by high-performance components including signal converters and digital processing circuits based on superconductive RSFQ technology.

7. ACKNOWLEDGMENT

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